cadence®

Interoperable Application-Specific Solutions for Formal Verification Throughout the Design Flow

The Cadence® JasperGold® Apps are a family of interoperable formal verification solutions—each of which is targeted at an individual verification application—that addresses formal verification challenges throughout the design flow. The JasperGold Apps approach not only eliminates much of the learning effort historically involved in the adoption and early-stage use of formal verification, but also provides an efficient method for deploying formal across the design team(s)[1].

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Introduction

Historically, formal verification technology has been licensed as a comprehensive suite of tools that can be used to address a broad range of formal verification applications and problems. Such deployment required a wide range of in-depth skills on the user's part before the technology could be leveraged by not only first time users, but also experienced ones. New users were often overwhelmed by the comprehensive nature of the technology and the steep learning curve, while experienced users wishing to deploy a narrow application scope across the organization were impeded by the all-in-one approach.

Early-stage users generally prefer to adopt and deploy new design and verification methods using a low-risk, step-by-step approach, which also allows them to accumulate skills and expertise incrementally. Experienced formal users are more likely to utilize focused capabilities to tackle specific issues and applications within design and verification, but must do so across an organization rather than on an individual basis. In both cases, users traditionally had to license an entire tool suite in order to access only a subset of its capability. Consequently, the all-in-one approach did not and does not provide for efficient deployment for either type of user.

Rather than deploying a general-purpose, all-in-one tool suite, many design teams need application-specific solutions that:

- Address a wide variety of verification applications throughout the design flow, enabling them to adopt formal technology, application by application
- Enable teams to acquire the expertise necessary to address only the verification task(s) in hand
- Allow teams to license only the technology appropriate for a particular application
- Eliminate or significantly mitigate the perceived risk in adopting unfamiliar technology

Moreover, these application-specific solutions must be interoperable, allowing design teams to mix and match them to meet task requirements and make maximum use of available budget. Ultimately, interoperability enables design teams to incrementally build an integrated tool suite, tailored to its particular needs. Clearly, design teams need interoperable application-specific solutions that address verification challenges throughout the design flow.

JasperGold Apps Solutions

JasperGold Apps fulfill the foregoing requirements. They are interoperable solutions, each of which targets an individual formal verification application. Using JasperGold Apps, design teams can adopt and expand their use of formal verification by employing a low-risk, application-by-application approach.

Each JasperGold App provides all of the tool functionality and formal methodology necessary to perform its intended application-specific task, eliminating the need to license a complete formal verification suite. Each JasperGold App enables the user to acquire only the expertise necessary for the particular task at hand, eliminating the need to become expert in every aspect of formal verification.

In addition, the JasperGold Apps' flexible licensing model enables design teams to optimize license usage by, for example, processing several instances of an App in parallel on different functional blocks, or executing several different Apps simultaneously on the same functional block.

JasperGold Apps Throughout the Design Flow

The JasperGold Apps family of interoperable solutions addresses formal verification applications throughout the design flow. For example, JasperGold Apps are used at the front end, to explore, verify, and debug architectural level models; in the middle to help develop and verify RTL blocks; and at the back end for post- silicon debug. Thus, the Apps afford adopters and early-stage users a broad and growing choice of application entry points in the design flow for their adoption and expanded use of formal verification.

The JasperGold Apps inter-operate via a single, common database that captures the results of all Apps/tasks, together with a common GUI that accesses only the data of interest to any given user. This tool architecture is essential not only for mixing-and-matching Apps, but also for the seamless enhancement of the JasperGold Apps family with additional Apps.

The JasperGold Apps Family

JasperGold Apps are currently available for formal property verification, behavior property synthesis, structural property synthesis, X-propagation verification, control/status register verification, connectivity verification, design coverage verification, sequential equivalence checking, low-power verification, security path verification, coverage unreachability analysis, and architecture modeling.

JasperGold FPV App

The JasperGold Formal Property Verification (FPV) App fully validates block-level properties and high-level requirements. It performs exhaustive and complete verification, and provides end-to-end full proofs of expected design behavior, as well as rapid bug detection. The App ensures the highest confidence possible in design functionality. The App is also used in:

- SoC integration, where it can be used to verify asynchronous clocking effects, arbitration, token leakage, dropped or corrupted data packets, cache coherency, etc.
- Post-silicon debug, where it identifies the failure scenario starting from the extracted failure trace, then validates the subsequent fix.

JasperGold BPS App

The JasperGold Behavioral Property Synthesis (BPS) App increases productivity and reduces time to market by generating assertions, constraints, and covers using the RTL and the existing simulation results obtained from batch simulations (FSDB/VCD) or interactive simulation (PLI). The JasperGold BPS App is unique in its ability to create white-box and black-box properties as well as temporal multi-cycle properties. In addition, the JasperGold BPS App can synthesize properties for signals from different modules across different levels of hierarchy. As with the JasperGold SPS App, the JasperGold BPS App provides an automated method for ranking and pre-classifying properties. The JasperGold BPS App ranks synthesized properties according to their added functional verification value compared to design and manually written assertions, to reduce the number of property candidates the

engineer must review. Moreover, the JasperGold Apps methodology provides a unique flow that allows engineers to combine the JasperGold BPS App and other JasperGold Apps to speed formal verification that significantly increases formal proof convergence. The JasperGold BPS App supports both VCD and FSDB/VCD file formats.

JasperGold SPS App

The JasperGold Structural Property Synthesis (SPS) App is used early in the validation process without the need to write a testbench or provide any stimuli. The structural properties are extracted from the RTL semantics and are used in early RTL development as well as RTL signoff. These structural properties can be configured from a wide variety of pre-defined functional checks such as dead code checks, FSM checks, arithmetic overflow checks, etc. The JasperGold SPS App is tightly integrated with the entire set of JasperGold Apps, drastically reducing the amount of checks that go undetected, un-proven, and un-diagnosed. Properties can be ranked, pre-classified, and output in standard SystemVerilog Assertions (SVA), which can then be used in any assertion-based verification (ABV) flow such as simulation, formal analysis, or emulation to increase functional coverage and reduce debug time. The JasperGold SPS App provides a fully automated flow to identify and generate checks without the need to annotate the RTL.

JasperGold XPROP App

The JasperGold X-Propagation Verification (XPROP) App enables the low-risk use of X's by design engineers and verification engineers for their own different purposes. It performs 2-state X-analysis and X-verification, enabling users to identify unintended X-propagation that can trigger undesirable behavior. It detects errors arising from the mismatch between a logic optimization X (meaning "don't care") and a verification X (meaning "unknown").

JasperGold CSR App

The JasperGold Control/Status Register Verification (CSR) App formally verifies control and status registers to exhaustively verify that the RTL conforms to the CSR definition, and that the attributes for a register and fields within a register are always correct. Applied to IP integration, the App performs checks at the block level, the unit level, and the chip level.

JasperGold CONN App

The JasperGold Connectivity Verification (CONN) App exhaustively verifies RTL connections at the block, unit, and chip level for IP integration. Using the design's connectivity table, it automatically generates the large number of properties (often thousands) necessary to verify complex connectivity in modern designs, significantly reducing effort and increasing productivity.

JasperGold COV App

Providing an empirical measurement on the effectiveness and progress of the formal verification, the JasperGold Design Coverage Verification (COV) App takes in the user's RTL, assertion properties, and constraint properties, and outputs a textual and GUI-based report showing how aspects of the DUT were verified by formal analysis. These reports show lines of code ("statement coverage"), conditional statements ("branch coverage"), and functional coverage points that were exercised.

JasperGold SEC App

Designed with high-productivity workflows, the JasperGold Sequential Equivalence Checking (SEC) App is a formal verification product that inputs two RTL files and verifies their sequential behavioral equivalence. The App delivers up to 10X faster runtimes compared to using regular formal tools.

JasperGold LPV App

Enabling exhaustive verification of design functionality with static and dynamic power optimization techniques, the JasperGold Low-Power Verification (LPV) App is the only dedicated formal solution for low-power functional verification. Unlike non-exhaustive simulation-based approaches, the JasperGold LPV App automatically generates assertions that verify that the power description matches the power intent and guidelines specifications (in IEEE 1801 standard Unified Power Format (UPF) or Si2's Common Power Format (CPF)). Then, the app exhaustively verifies that the power modifications did not create any new hazards and are consistent and correct.

JasperGold SPV App

Developed with unique path sensitization technology, the JasperGold Security Path Verification (SPV) App is a formal verification product that accepts RTL containing a specific secure area (memory or registers). The App exhaustively proves that secure data can't be read illegally (no leaks), can't be illegally overwritten (sanctity), and remains secure in the face of faults or failure

JasperGold UNR App

Automating the previously tedious, time-consuming code coverage analysis process, the JasperGold Coverage Unreachability (UNR) App saves weeks of time to attain verification closure. The app takes partially complete simulation coverage database and RTL code for the DUT as inputs, and automatically generates properties to formally explore the reachability of uncovered cover points remaining in the database. The app can be readily used by simulation users with minimal formal verification experience.

JasperGold ARCH App

The JasperGold Architectural Modeling (ARCH) App helps the design team to create and verify an executable specification of circuit functionality, offering architectural-level visibility of functional behavior prior to RTL implementation. The App generates properties from the executable spec, with which the downstream RTL can be formally verified. An example of the App's use is the exhaustive verification of complex protocols such as the latest on-chip interconnect specifications and cache protocols.

Summary

The Cadence JasperGold Apps family of interoperable application-specific solutions addresses a wide variety of verification applications, enabling design teams to adopt and apply formal technology at any point in the design flow. Specifically, they:

- Enable users to acquire the expertise necessary to address only the verification task(s) in hand, eliminating the need to develop a wide range of in-depth skills
- Allow users to license only the technology appropriate for specific applications, eliminating the need to license a complete formal verification suite
- Reduce perceived adoption and deployment risk by enabling design teams to deploy formal verification incrementally—one application at a time
- Offer the flexibility to mix and match Apps to meet task requirements and make maximum use of available budget
- Incrementally build an integrated tool suite, tailored to the design team's particular needs
- Allow seamless integration between the Apps not only to share information and work but also to leverage work done at all stages of the design and verification

The JasperGold Apps approach offers more than technology—it offers formal verification solutions that address verification challenges throughout the design flow.

References and Further Information

[1.] We need a simpler and faster approach to formal verification! by Rajeev Ranjan. EE Times, 30 July 2012.

To learn more about Cadence JasperGold Apps, contact your local sales office at http://www.cadence.com/cadence/contact_us.

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