

# Welcome to

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February 24–26, 2026  
Santa Clara Convention Center

## Expo

February 25–26, 2026



# A Case Study on JESD204C Signal Integrity Compliance

Garrett Warren, Mercury Systems

Shawn Mills, Cadence Design Systems



# SPEAKERS



## Garrett Warren

*Electrical Engineer III, Mercury Systems*

[garrett.warren@mrcy.com](mailto:garrett.warren@mrcy.com) |

Garrett Warren is an Electrical Engineer at Mercury Systems focused on microelectronics package design. He has over 4 years of experience in the architecture, design, and simulation of advanced system-in-package devices and verification platforms. Garrett received his BSE in Electrical Engineering from Arizona State University and is currently working on his MSE at ASU with a focus in electromagnetics and microwave circuit design.



## Shawn Mills

*Principal SI/PI Applications Engineer, Cadence Design Systems*

[shawnm@cadence.com](mailto:shawnm@cadence.com)

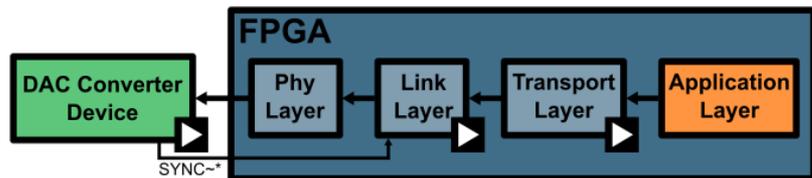
Shawn Mills is a Principal SI/PI Applications Engineer at Cadence Design Systems focusing on layout and system level analysis. He has over 10yrs of experience in the design, modeling, analysis, and design of mixed signal circuits. He has completed his BSE and MSE in electrical engineering at Arizona State University. In addition to Cadence, Shawn has held engineering roles at Raytheon, General Dynamics, Mercury Systems and has 10yrs military experience.



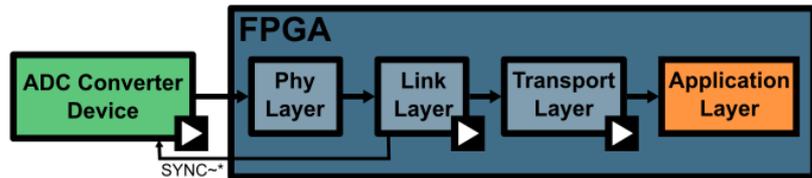
# Agenda

- History of JESD204 protocol (204A-C)
- Applications of JESD204C and JESD204C IP
- JESD204C Design Guidelines and Simulation in Cadence Tools
- JESD204C Verification
- Future applications/advancements
- Sigrity/Clarity flow for Heterogenous Integration
- SystemSI for UClE Compliance Checking
- Summary

## JESD204B/C TX Chain



## JESD204B/C RX Chain



External hardware components

Standard HDL components

Application specific user-defined HDL component

\* SYNC~ present in JESD204B only

Source: Analog Devices



# History/Overview of JESD204

- JEDEC Standard JESD204X: Serial Interface for Data Converters
  - X = placeholder for JESD204 revision (A-D)
- Used for high-speed ADC/DAC to FPGA/ASIC communication
- Normally used as package-to-package interface but can also be configured as die-to-die (D2D) interface
- Leverages IEEE 802.3 ethernet standard for core functionality

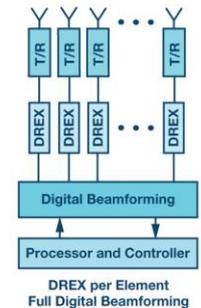
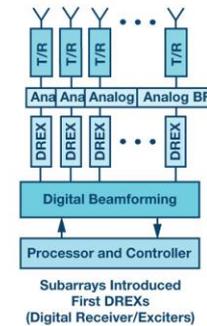
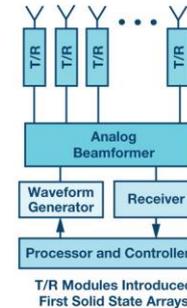
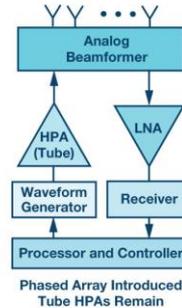
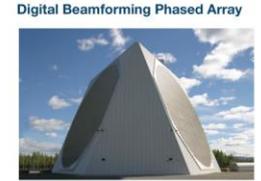
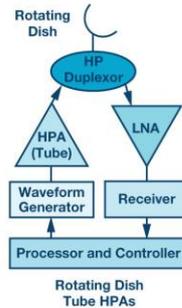
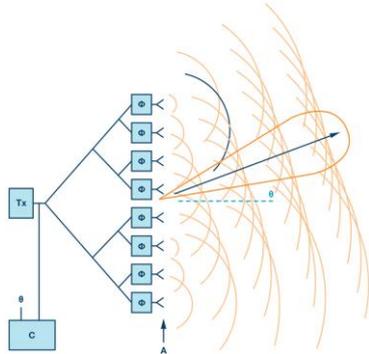
Feature	JESD204A	JESD204B	JESD204C	JESD204D
Release Date	April 2008	July 2011	February 2017	April 2021
Max Lane Rate	3.125 Gbps NRZ	12.5 Gbps NRZ	32 Gbps NRZ	112 Gbps PAM4
Signal Type	NRZ	NRZ	NRZ	PAM4
Encoding	8b/10b	8b/10b	64b/66b	64b/66b
Deterministic Latency	No	Yes	Yes	Yes
Synchronization	SYNC	SYNC~	SYNC~ & SYSREF	Enhanced SYNC~ & SYSREF
Forward Error Correction	No	No	Optional	Optional
Multi-Device Sync	Limited	SYSREF-based	SYSREF-based	Enhanced SYSREF
Typical Efficiency	80%	80%	97%	97%
Link Configuration	Static	Static	Dynamic	Dynamic

Source: JESD204C Standard



# Applications of JESD204

- Multi-channel data acquisition
- Beam forming
- Radar
- Electronic Warfare
- Wireless Communications
- Many more!



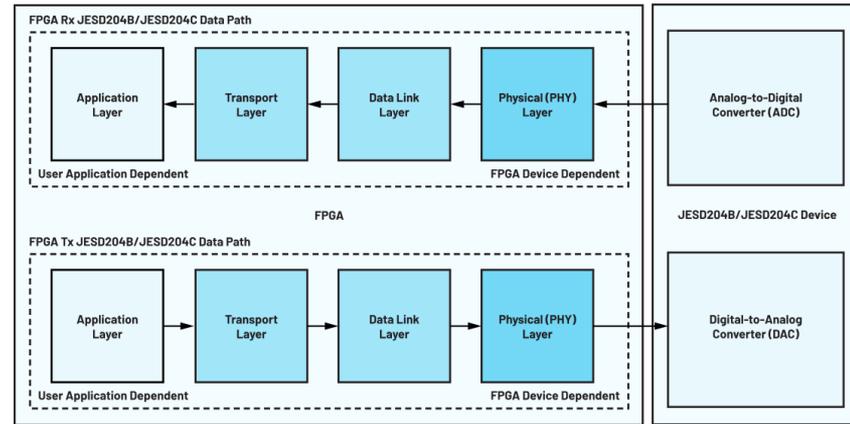
Source: Analog Devices



# Basics of JESD Operation

Source: Analog Devices

- Focus of this presentation is on physical (PHY) layer
- Readily available IP for SoCs (e.g. AMD Versal platform)
- SYSREF: periodic signal used to align boundaries of local clocks
  - Source synchronous with device clock
- JESD204C compliance assessed through channel operating margin (COM)



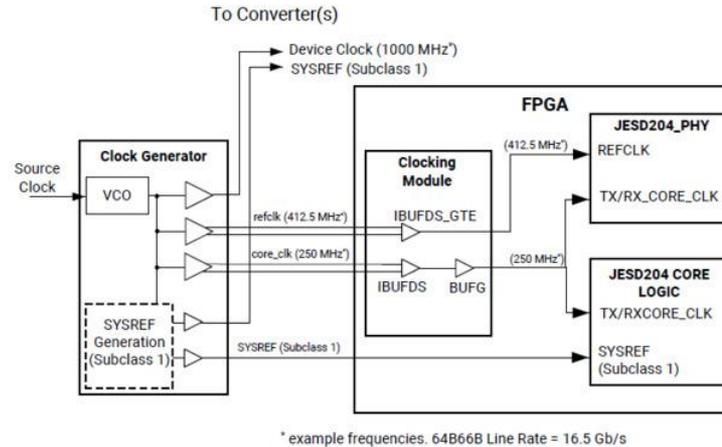
Class	Relative Power	Transmitter FFE (Minimum)	Receiver CTLE (Minimum)	Receiver DFE Taps (Minimum)
C-S	Low	9.5 dB	6 dB	0
C-M	Medium	9.5 dB	9 dB	3
C-R	High	9.5 dB	12 dB	14



# JESD204C Design Considerations

- IP Support: Can a selected FPGA and ADC/DAC die communicate with each other and is IP available?
- PRBS Generator/Checker features for D2D applications
- SYSREF/Clocking Distribution
  - Requires JESD204X compliant clock generators
- Skew Budget
  - Intra-link and Inter-link skews
    - *Transmission: physical propagation delays*
    - *Processing: skew inside TX/RX devices*
    - *Timing Reference: skew due to different arrival times for SYSREF and SYNC*
- AC/DC Compliant Devices?
  - Typically utilize on-package AC coupling capacitors

Figure 3: Separate Transceiver Reference and Core Clocks: 64B66B Example for UltraScale+/UltraScale Devices

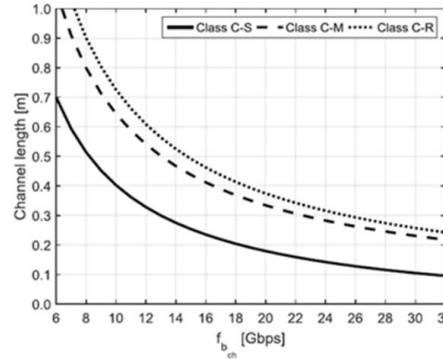


Source: AMD PG198 JESD204 PHY

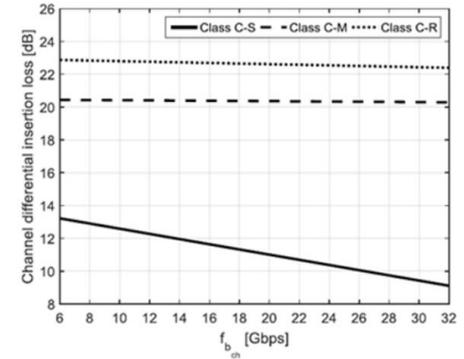


# JESD204 Compliance Rules

- JESD204B specifies following:
    - Differential Insertion Loss Masks
    - Differential Return Loss Masks
    - Transmit/Receive Eye Masks
  - JESD204C adjusts compliance to focus on:
    - COM of at least 2dB at BER of 10e-15
    - Differential IL/RL Masks
    - Skew and Latency Variation Budgets
- *Measured at multiple points along channel*



(a) channel length ( $l_{ch}$ )



(b) differential insertion loss at the Nyquist frequency ( $IL_{ch}$ )

Source: JESD204C Standard



# Cadence SystemSI Solution

- JES204B/C compliance verification using Sigrity System SI
  - Allows for custom compliance kit creation or built-in compliance kits for UCIe, PCIe Gen 3-6, etc.
- Able to setup custom or use existing compliance items for:
  - Eye Masks
  - Differential Insertion/Return Loss Masks
  - COM
  - Insertion Loss Deviation (ILD)
  - Skew Budget
  - Stressed/Swept Jitter

### JESD204C Compliance Kit

This Compliance Kit will check the Differential Insertion Loss (IL), Insertion Loss Deviation (ILD), TX Eye Mask, RX Eye Mask, COM for the JESD204, 32.5Gbps.

#### Choose Compliance Items

No.	Parameter	Values	■
<b>Tx Tests</b>			
1	Tx Eye Mask (at BER=1e-12)	Mask File: ...2p5_TX_mask.maskfil Edit...	<input checked="" type="checkbox"/>
2	Tx Signal to Noise Distortion (at BER=1e-12)	32.5 dB	<input type="checkbox"/>
<b>Rx Tests</b>			
3	Eye Height (at BER=1e-12)	200 mV	<input type="checkbox"/>
4	Eye Width (at BER=1e-12)	0.5 UI	<input type="checkbox"/>
5	Eye Mask (at BER=1e-12)	Mask File: ...RX_eye_mask.maskfil Edit...	<input checked="" type="checkbox"/>
6	COM (at BER=1e-12)	2 dB	<input type="checkbox"/>
<b>Skew Budget</b>			
7	Lane-to-Lane Skew	5 ns	<input type="checkbox"/>
8	Skew between P and N Side of Thru Diff Pair	10 ps	<input type="checkbox"/>
<b>Differential Insertion Loss</b>			
9	Insertion Loss Setup...	Mask File: ...2p5_il_mask.maskfil Edit...	<input checked="" type="checkbox"/>
10	ILD Setup...	Mask File: ...p5_ild_mask.maskfil Edit...	<input checked="" type="checkbox"/>
11	ICR Setup...	Mask File: ...generic_icr.maskfile Edit...	<input type="checkbox"/>
<b>Differential Return Loss</b>			
12	Tx Return Loss Setup...	Mask File: ...TX_RL_mask.maskfil Edit...	<input checked="" type="checkbox"/>
13	Rx Return Loss Setup...	Mask File: ...RX_RL_mask.maskfil Edit...	<input checked="" type="checkbox"/>
14	Effective Return Loss	11.9 dB	<input type="checkbox"/>
<b>Stressed/Swept Jitter Test</b>			
15	Stressed/Swept Jitter (at BER=1e-12)	Mask File: ...olmask\olmask.txt Edit...	<input type="checkbox"/>



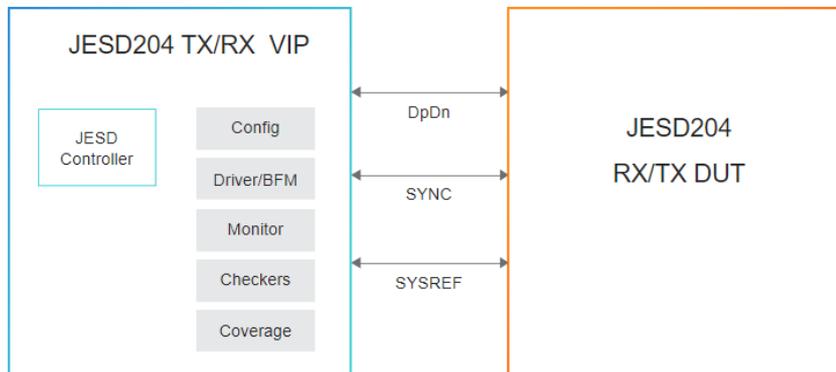
# Prerequisites/Setup

## Model Availability

- IBIS-AMI models from chiplet/package vendors
- S-parameters extracted for organic package and/or PCB(s) depending on application

## Review Artifacts

- Stackup review
- Material properties review
- BOM/component review
- Layout DRC checks
  - Trace spacing
  - Length matching
  - Impedance control (typically 100 Ohms differential)



The screenshot shows the Cadence Cross-section Editor interface. On the left is a table with columns for Objects, Types, Thickness, Physical, Embedded, and Signal Integrity. On the right is a cross-section diagram showing the physical layers of the PCB stackup.

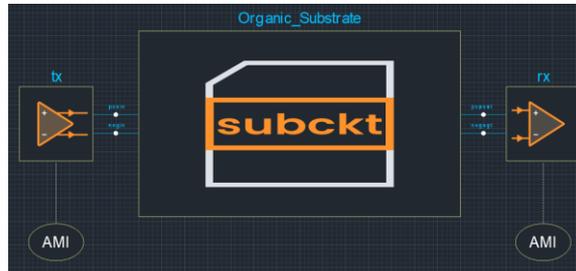
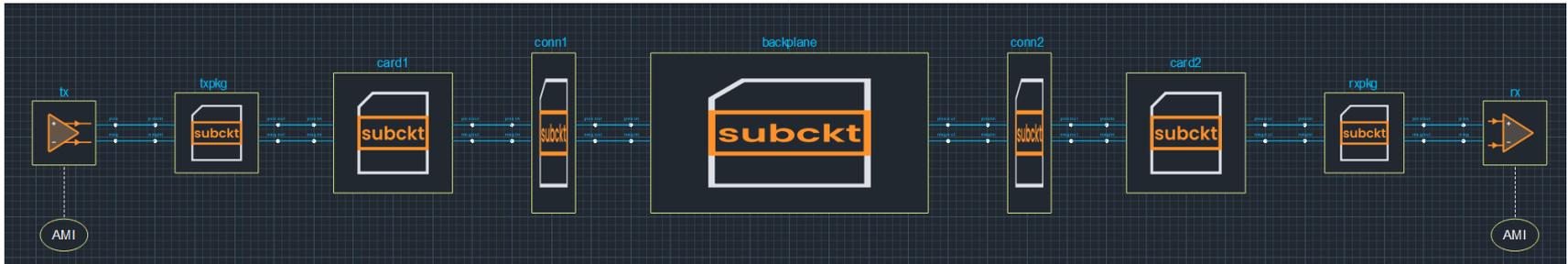
Objects	Types	Thickness	Physical	Embedded	Signal Integrity			
#	Name	Layer	Layer Function	Value mil	Layer ID	Material	Embedded Status	Conductivity mho/cm
*	*	*	*	*	*	*	*	*
		Surface						
	Silkscreen_Top	Mask	Silkscreen	2		Polyimide		0
	Soldermask_Top	Mask	Solder Mask	2		Polyimide		0
1	Top	Conductor	Conductor	0.7	1	Copper	Not embedded	595900
		Dielectric	Dielectric Prepreg	8		Fr-4		0
2	Gnd	Plane	Plane	1.2	2	Copper	Not embedded	595900
		Dielectric	Dielectric Core	43		Fr-4		0
3	Vcc	Plane	Plane	1.2	3	Copper	Not embedded	595900
		Dielectric	Dielectric Prepreg	8		Fr-4		0

Source: Cadence



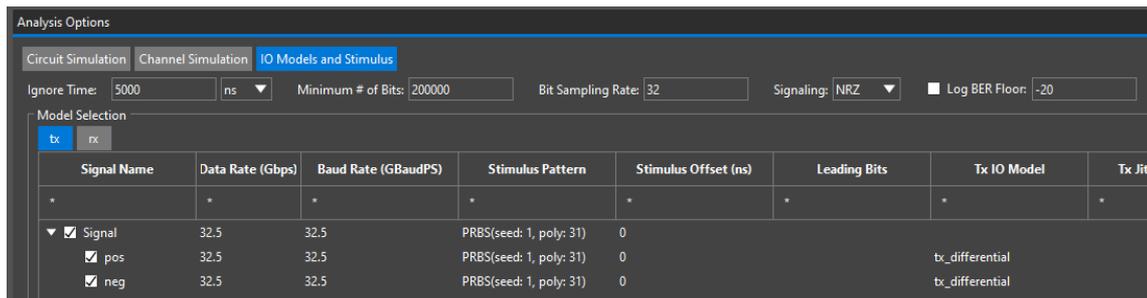
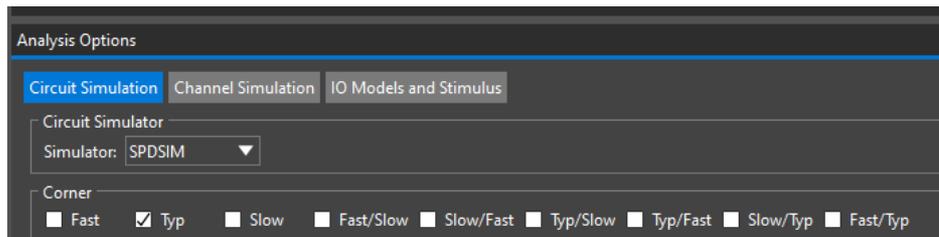
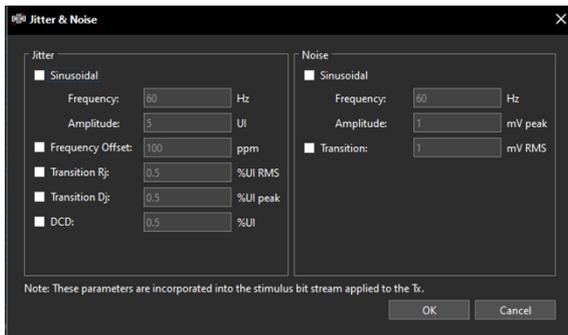
# SystemSI Simulation Setup

- System level implementation shown (including PCBs)
  - Can also be modified for die-to-die application including substrate s-parameters



# SystemSI Simulation Setup (continued)

- Simulation Parameters setup including:
  - Corners
  - # of bits
  - Signaling mode (NRZ up to PAM8)
  - Data rate
  - Stimulus pattern (e.g., PRBS31)
  - Injected Jitter/Noise



# SystemSI Compliance Report

- Provides clear PASS/FAIL data and corresponding time/frequency domain waveforms

**JESD204C Compliance Report**

Generated by Topology Workbench, Cadence Design Systems Inc.,  
Jan 13, 2026

This Compliance Kit will check the Differential Insertion Loss (IL), Inertial Loss Deviation (ILD), TX Eye Mask, RX Eye Mask, COM for the JESD204, 32.5Gbps.

**Useful Links**

- Cadence website: <http://www.cadence.com>

**General Information**

- Project File: jcom\_kit.topx
- Circuit Simulator: SPDSIM

**Summary of Results**

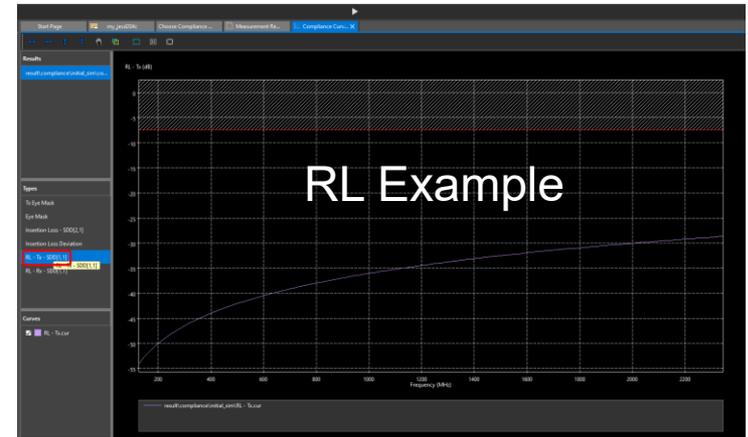
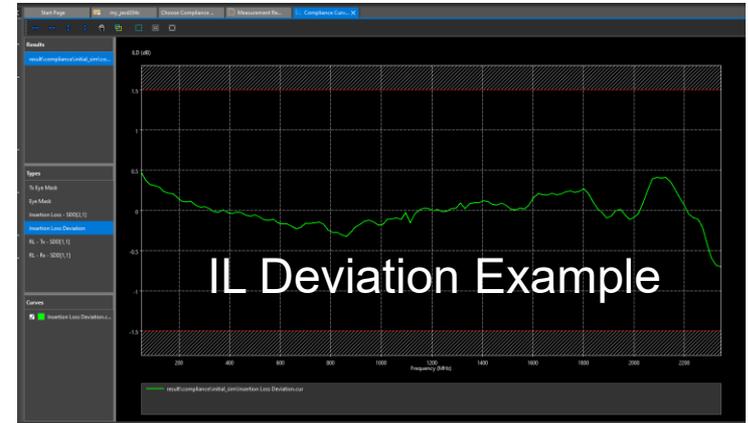
This report shows the results of the compliance testing using Cadence TopXp. The channel simulated violates one or more compliance requirements.

**Tx Tests**

Item	Value	Simulation Results	Pass/Fail
Tx Signal to Noise Distortion Ratio (SNDR) (at BER=1e-12)	32.5 dB	109.678 dB	Pass

**Rx Tests**

Item	Value	Simulation Results	Pass/Fail
Eye Height (at BER=1e-12)	200 mV	320,000 mV	Fail
Eye Width (at BER=1e-12)	0.5 UI	0.670 UI	Fail
Eye Mask (at BER=1e-12)		Eye Mask	Pass
COM (at BER=1e-12)	2 dB	11.820 dB	Pass



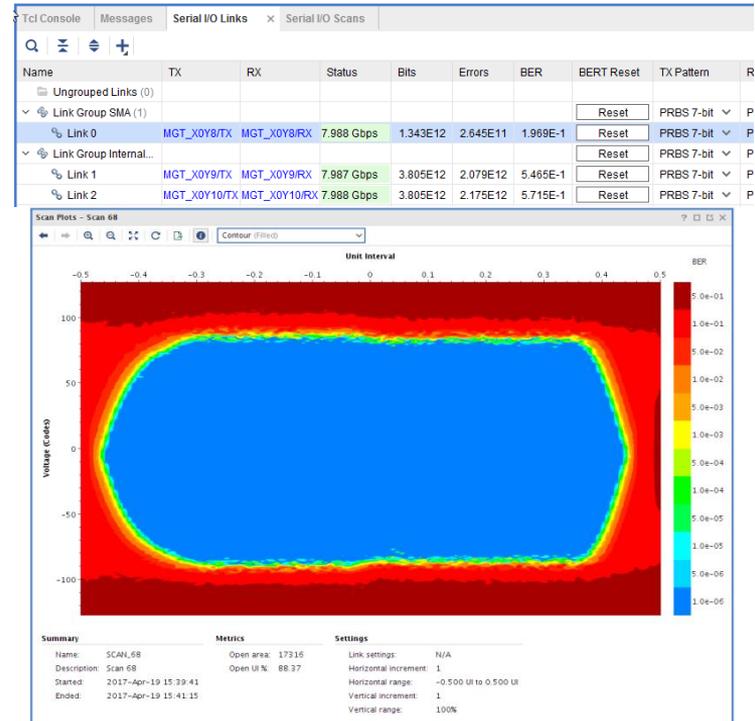
# JESD204C Verification & Test

## Challenges:

- On-package interfaces are buried with minimal test access
- IP compatibility between vendors

## Solutions

- IEEE 1149.6 boundary scan for differential signals
  - *IEEE 1149.1 configured for DC interconnects only*
- FPGA and ADC/DAC PRBS generators/checkers
  - *E.g., AMD Vivado IBERT*

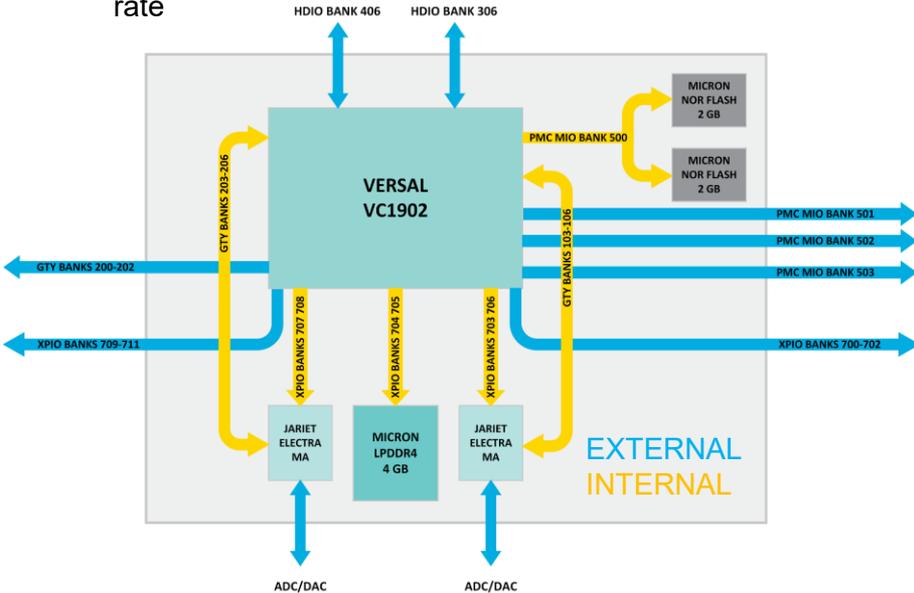
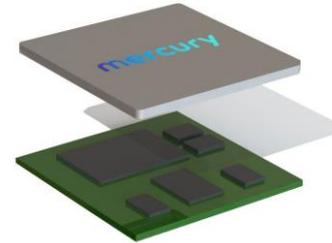


Note: IBERT examples shown for reference only. Do not represent real JESD204C channel.



# Real World Application: Mercury RFS1140

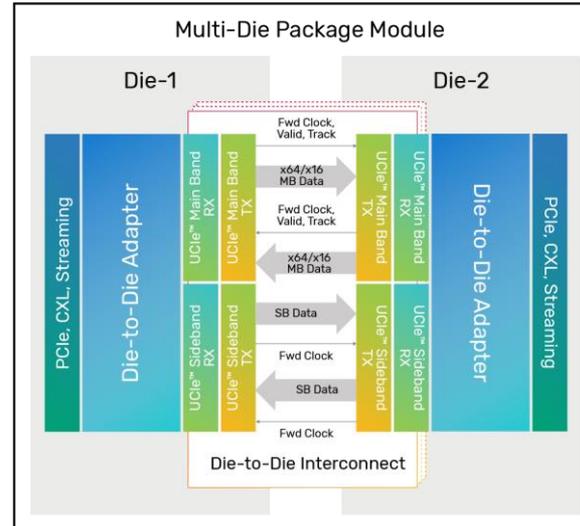
- Mercury RFSiP featuring AMD Versal VC1902 die and high-speed Jarriet Electra ADC/DAC chiplets
- Features JESD204C for FPGA to ADC/DAC communication with up to 64 GSPS RF sampling rate



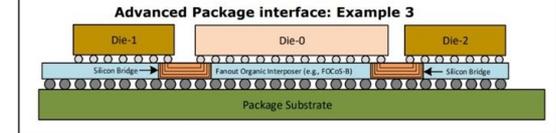
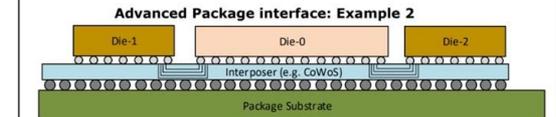
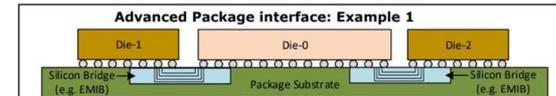
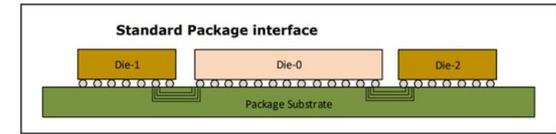
# Future Applications/Advancements

- JESD204D released in 2021 supporting up to 112 Gbps PAM4 per lane
- Many ADC/DAC vendors moving away from JESD204 protocol in cutting edge chiplets
- UCIe STD/ADV being architected as alternative interface

## Standard vs Advanced Package



Source: Cadence

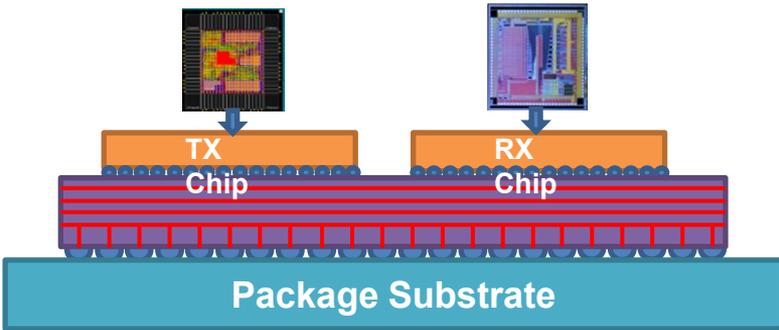
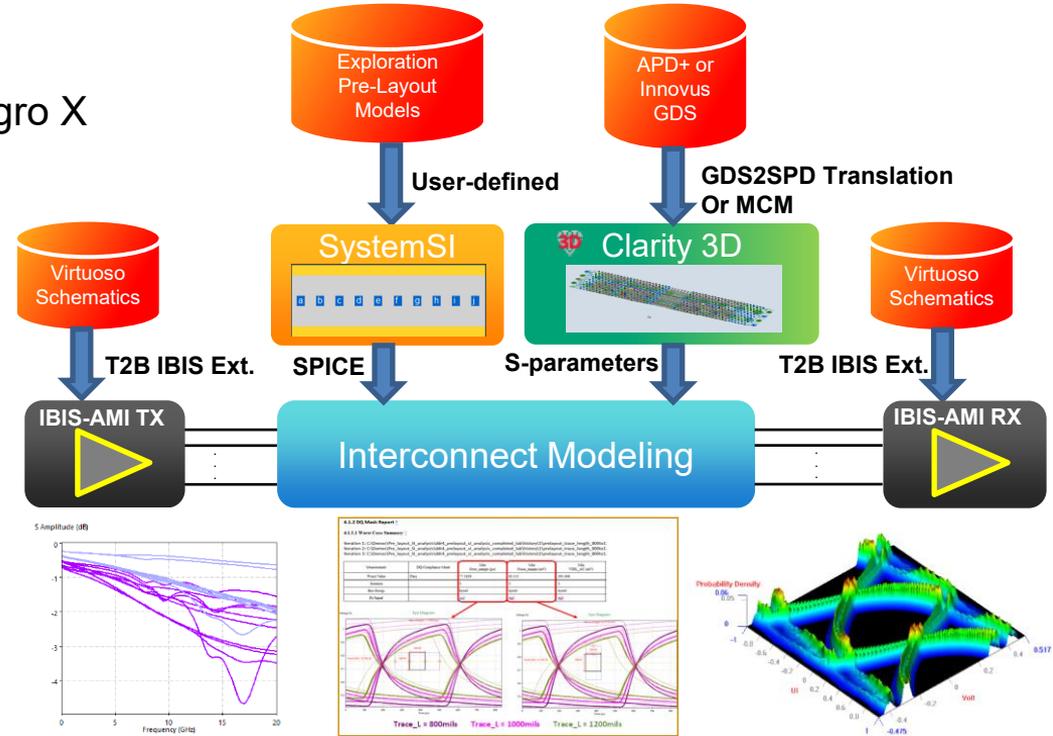


Source: UCIe Standard



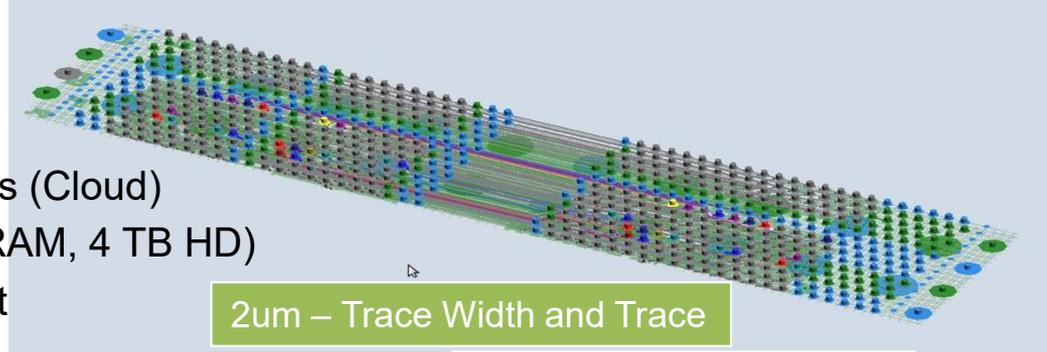
# Sigrity X SI flow for Heterogeneous Integration

- Three Platforms to cover Full Flow
  - Virtuoso, Sigrity X, Clarity, and Allegro X
- Exploration and Sign-off Portfolio
- Spec-driven Compliance Reports
- Analysis are Scalable with Core Count

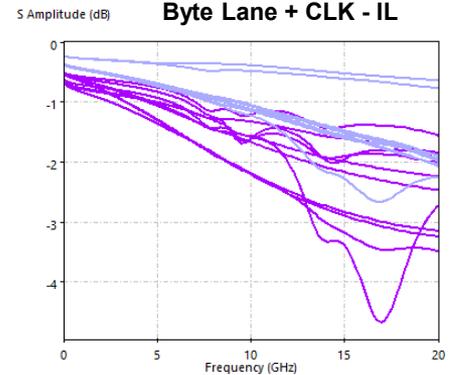
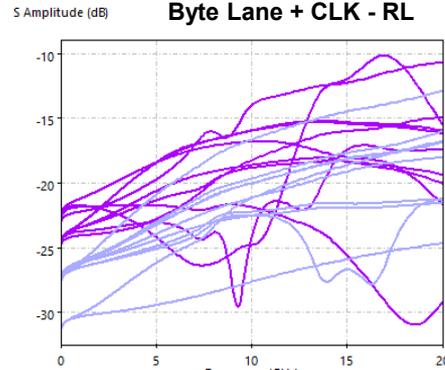
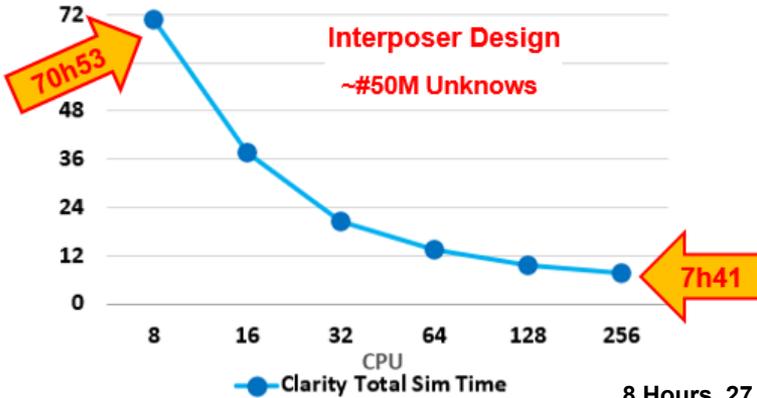


# Case Study - Full 3D Extraction of Interposer with Clarity

- 8 layers Silicon Interposer fully degassed
- 43 ports - 2 Byte Lanes + CLK signals
- Total Sim Time: 24 hours (local) to 8 hours (Cloud)
  - MS Azure Cloud (96 cores, 674GB RAM, 4 TB HD)
- Full 3D extraction scalable by Core Count



Clarity Total time – Scalability Profile



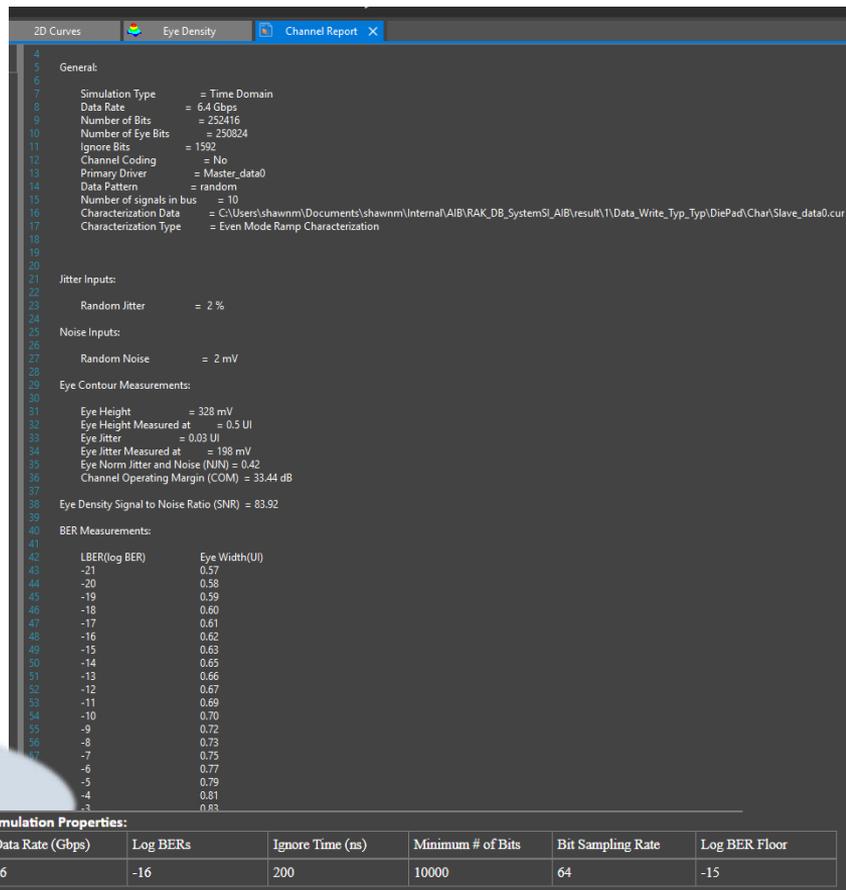
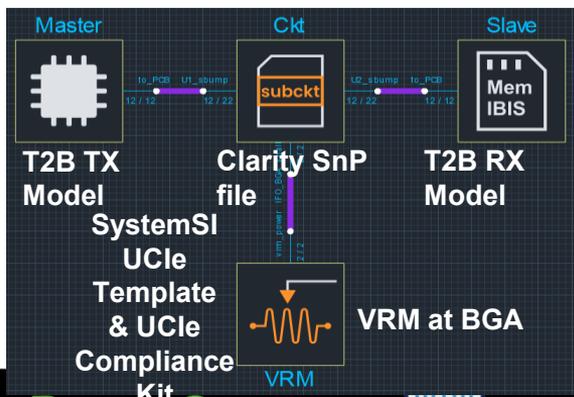
8 Hours, 27 Freq. Points, 6.7M Elements, 42M

Initial Mesh	Adaptive Mesh	# iterations	Final Sim.	Total Time	# Freqs.	# Elements	# Unknowns	# of Ports
3:18:53	0:48:26	9	3:50:19	7:58:28	27	6,680,968	41,669,160	43



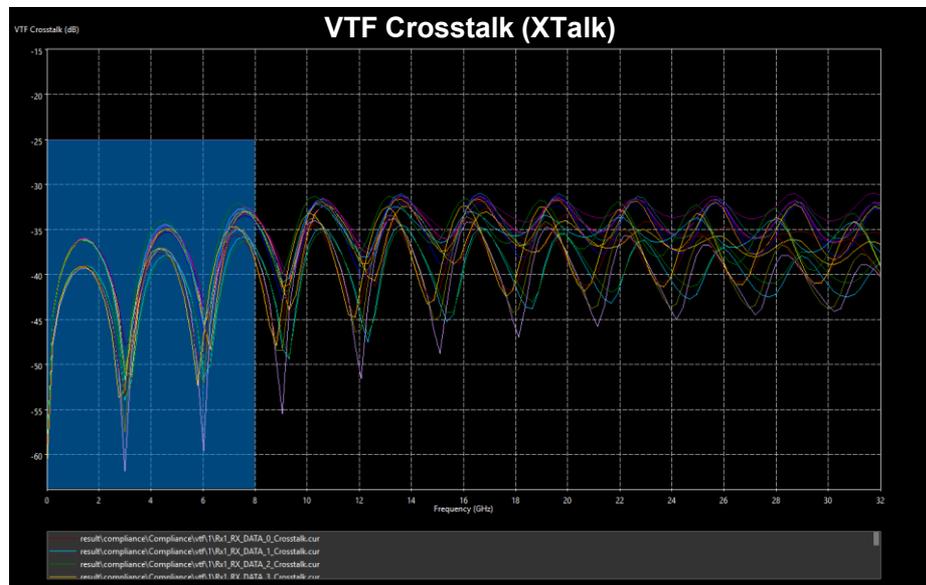
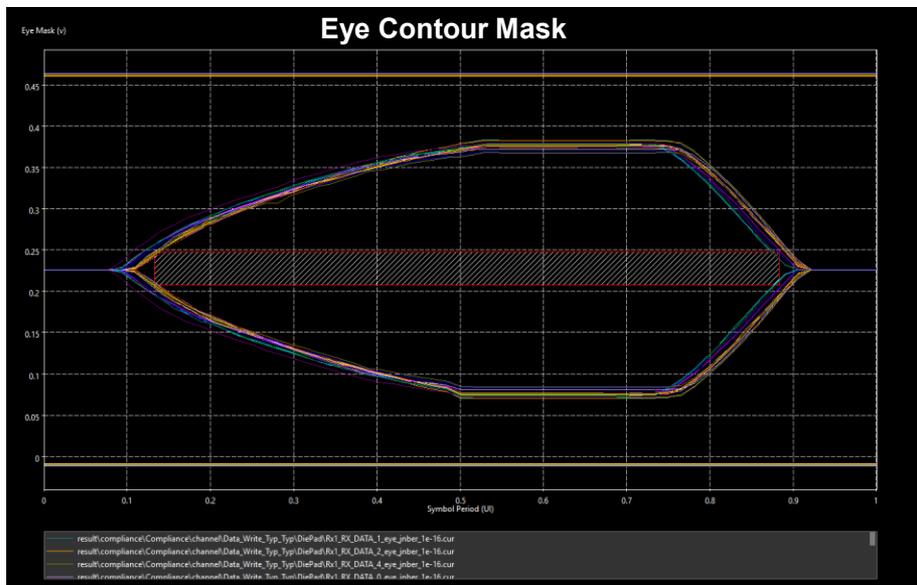
# Sigrity X SystemSI Simulation Results with Interposer Model

- Public Template for UCle Topology
- Supports SPICE or IBIS-AMI from T2B
- Multiple Types of Interconnects
  - Pre-layout, S-parameters, SPICE ckt, Clarity Layout Block
- Parametric Sweep and Optimization Available
  - Geometric and AMI parameters can be swept
- Spec-driven Compliance Report – 6.4Gbps



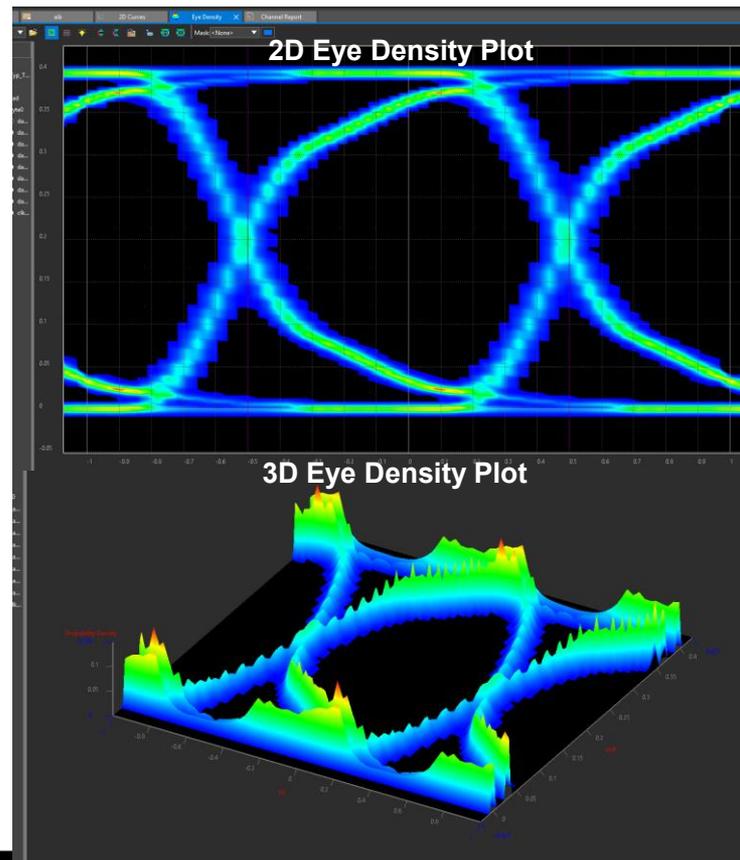
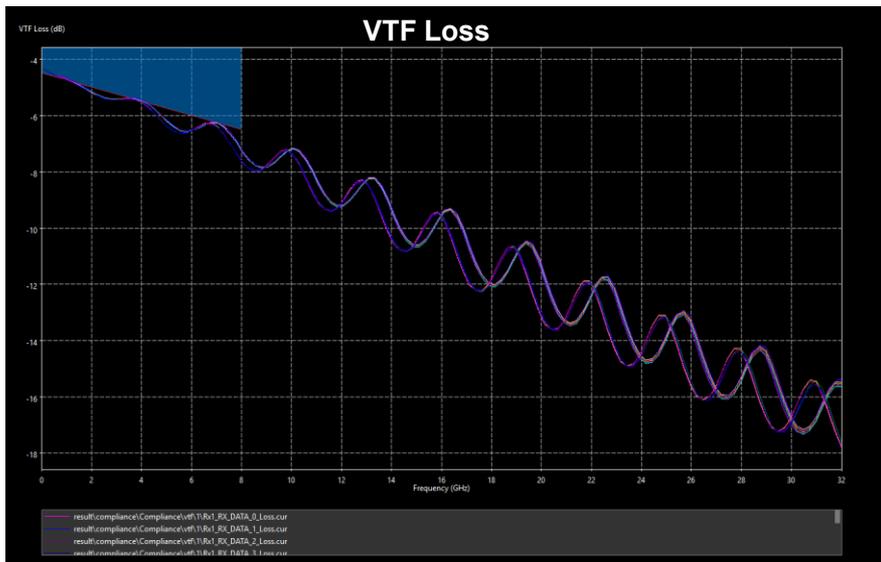
# SigrityX SystemSI UCle Simulation Results

- Easily Check & Verify Eye Contour with mask
- VTF Crosstalk



# SystemSI VTF Loss & Eye Density Simulation Results

- Easily Check & Verify VTF Loss
- 2D and 3D Eye Density Plots



# Summary

- SystemSI offers a complete “system-level” analysis solution
  - Multiple input formats in both time and frequency domain for ICs, PKGs and PCBs
- Cadence SigrityX, Clarity, Allegro X and Virtuoso platforms comprise Full flow from design to analysis
  - JESD204C Custom Compliance
  - UClc, PCIe3,4,5,6, and many others for standards compliance checking with templates
- Use Clarity for Full 3D Extraction for an multiple design fabrics (3DIC, POP, 2.5D, etc)
  - Cloud Service option (Microsoft Azure, Cadence Cloud, Nimbix Jarvice, others)
  - Scalable and High Capacity
- Easy-to-use JESD204C Custom Compliance Kit saved hours of engineering work to build a circuit test-bench
- Both Extractions and circuit simulation are scalable with Core Count
  - When transferring 960Gbps and/or larger data between chipelets....
  - Take Transmission Line effects seriously or risk the wrath of Heaviside



# Thank you!

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## QUESTIONS?

### **Garrett Warren**

*Electrical Engineer III, Mercury Systems*

[garrett.warren@mrcy.com](mailto:garrett.warren@mrcy.com) | [mrcy.com](http://mrcy.com)

### **Shawn Mills**

*Principal SI/PI AE, Cadence Design Systems*

[shawnm@cadence.com](mailto:shawnm@cadence.com) | [ASK Cadence](#)

