Welcome to

Conference
January 28–30, 2025
Santa Clara Convention Center

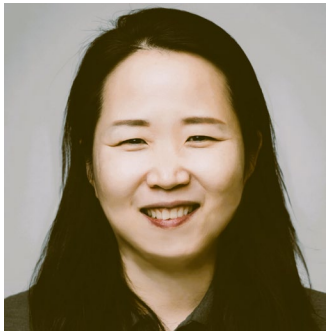
Expo
January 29–30, 2025

Accelerating Time-to-Market in the Chiplet Era

Chiplet architecture and case study focusing on security and system protection

Junie Um, (Cadence)
Samuel Wong, (Secure-IC)

SPEAKERS



Junie Um

Distinguished Engineer, Compute Solutions Group/SSG, Cadence

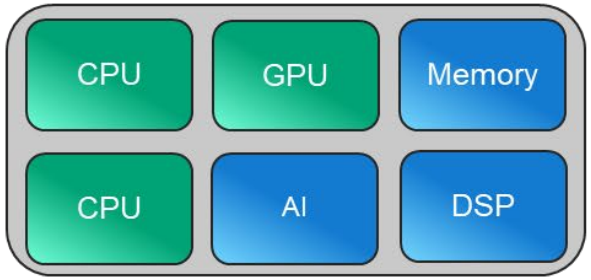
Junie Um has been working on system and SoC architecture for a series of mobile and ADAS SoCs. Currently, she is responsible for chiplet and ADAS system architecture at Cadence. She received a BS degree from Seoul National University and MS and PhD degrees from the Korea Advanced Institute of Science and Technology (KAIST). She also served as a visiting scholar at the University of Texas at Austin.

Samuel Wong

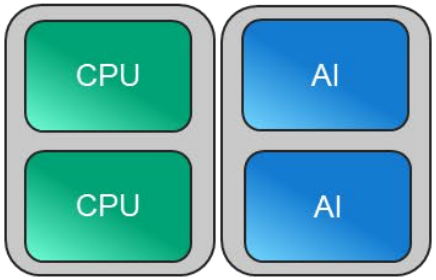
Business Development Manager, Secure-IC

Sam Wong leads business development and sales activities for Secure-IC, bringing over 20 years of experience in international business development and semiconductor IP licensing. He began his career at Arm in Austin, focusing on emerging markets and managing the Arm Foundry Program. Sam then leads Tensilica's APAC sales operations, playing a pivotal role in opening the China and Taiwan markets. He also serves in various roles at Boeing, NetSpeed, and an AI startup.

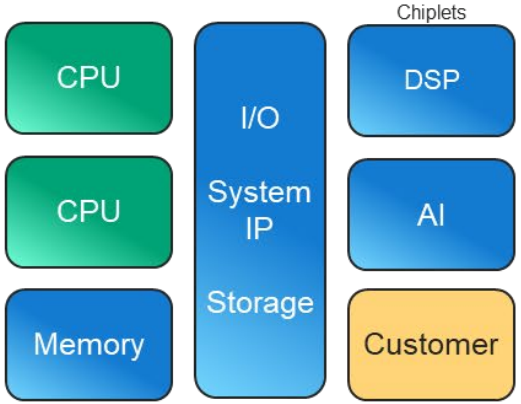
The Journey of a SoC designer



Heterogenous SoC
Differentiation



Multi-Die SoC
Maximize Die Area



Heterogeneous Chiplet System
Extreme Specialization

- Heterogenous SoCs
  - Single, monolithic die
  - Integration of IP with some specialized IP
- Designers look for ways to build bigger, faster, and cheaper systems
  - Multi-die solutions to build big
  - Multi-chiplet solutions to build faster and cheaper with more specialization

Monolithic Die

Why Chiplets? An Engineering Value Proposition

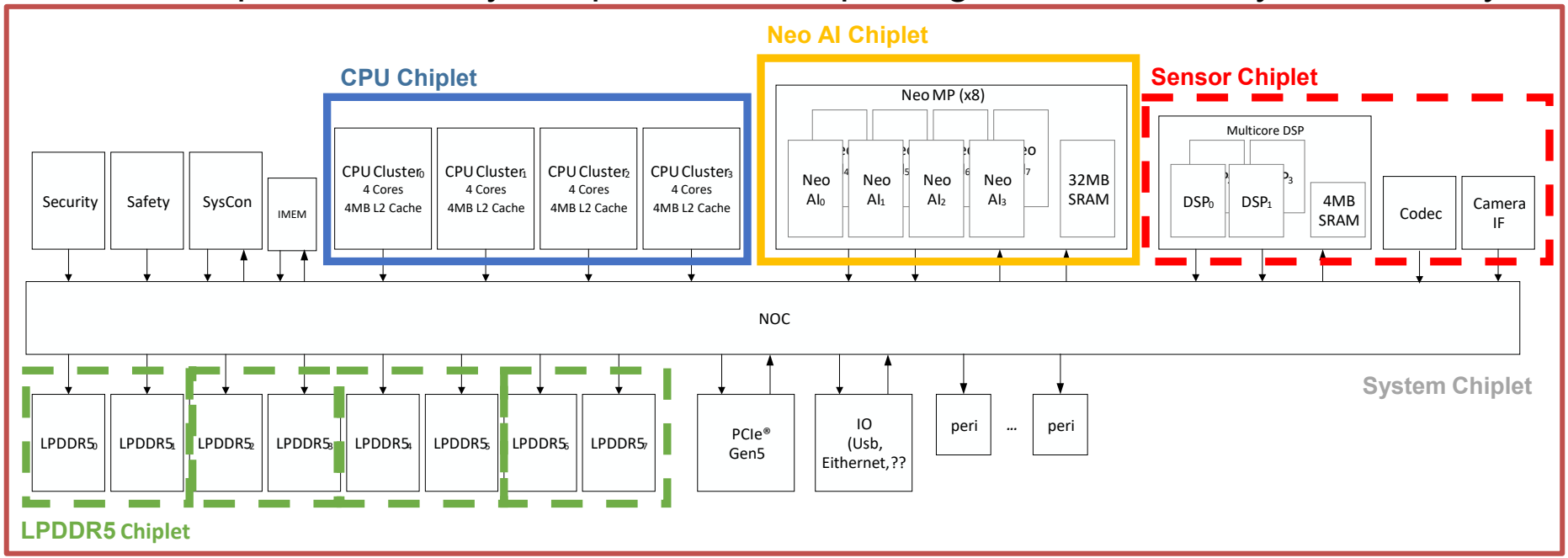
1. Cost-effectiveness and complexity efficiency
   - Focus engineering teams on unique value-add while improving time to market, project derisk, and costs
   - Leverage partners for advanced-node designs, IP, and software virtual platform
2. Modularity – Scalability and customizations
   - Enabling very large systems – *make it big* – multi-chip solutions
   - Scalable solutions from low- to high-end – *make it fast, make it cheap* – multi-chiplet solutions
3. Portfolio management
   - Develop product roadmaps built with the same chiplets
   - Reuse of select chiplets for next-generation products
4. Ecosystem development
   - Leverage software ecosystem around partner chiplets (reference design)
   - Utilize off-the-shelf chiplets (standard IP – CPU, GPU, memory, I/O)

Cadence Chiplet Development Efforts

- **Reference designs** to accelerate the design effort
  - Base System Chiplet – Tapeout completed in October 2024
  - Building NPU chiplet targeting Q3 2025
  - Continue to build a reference platform
  - Supporting configurable subsystem
- **Chiplet frameworks** to simplify chiplet construction
- Building **SoC cockpit** to accelerate the design effort
- Designing to support the **standard chiplet system architectures**
  - Joining standardization efforts
    - How chiplets interoperate – the behavior of chiplets
    - How chiplets communicate – data/event communication of chiplets

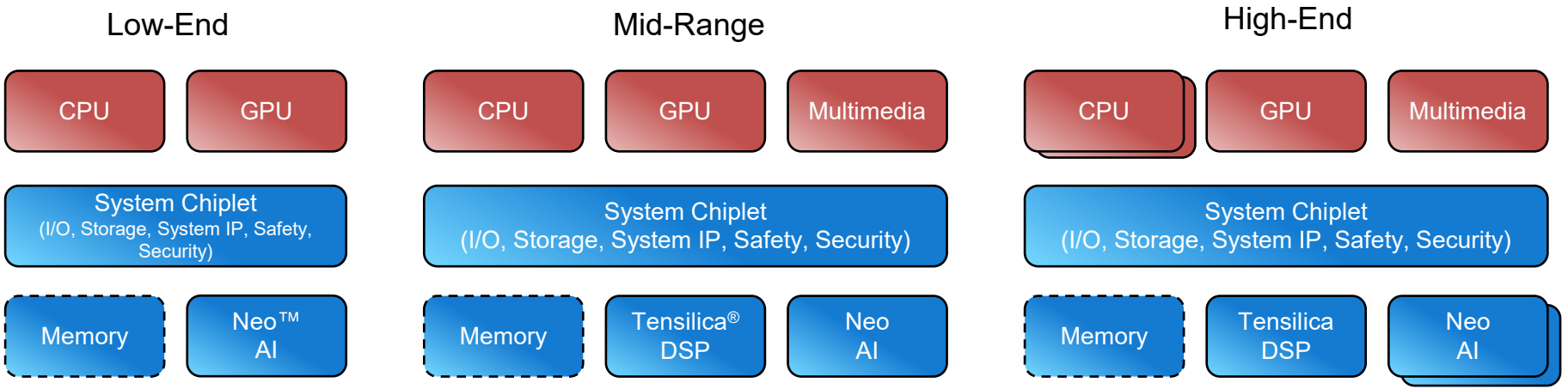
Example ADAS Chiplet Decomposition

- CPU, Cadence® Neo™ AI, system functions with optional sensor, memory, and I/O chiplets
- Tradeoff process cost, yield, performance, package cost, scalability, extensibility



ADAS Product Family with Chiplets

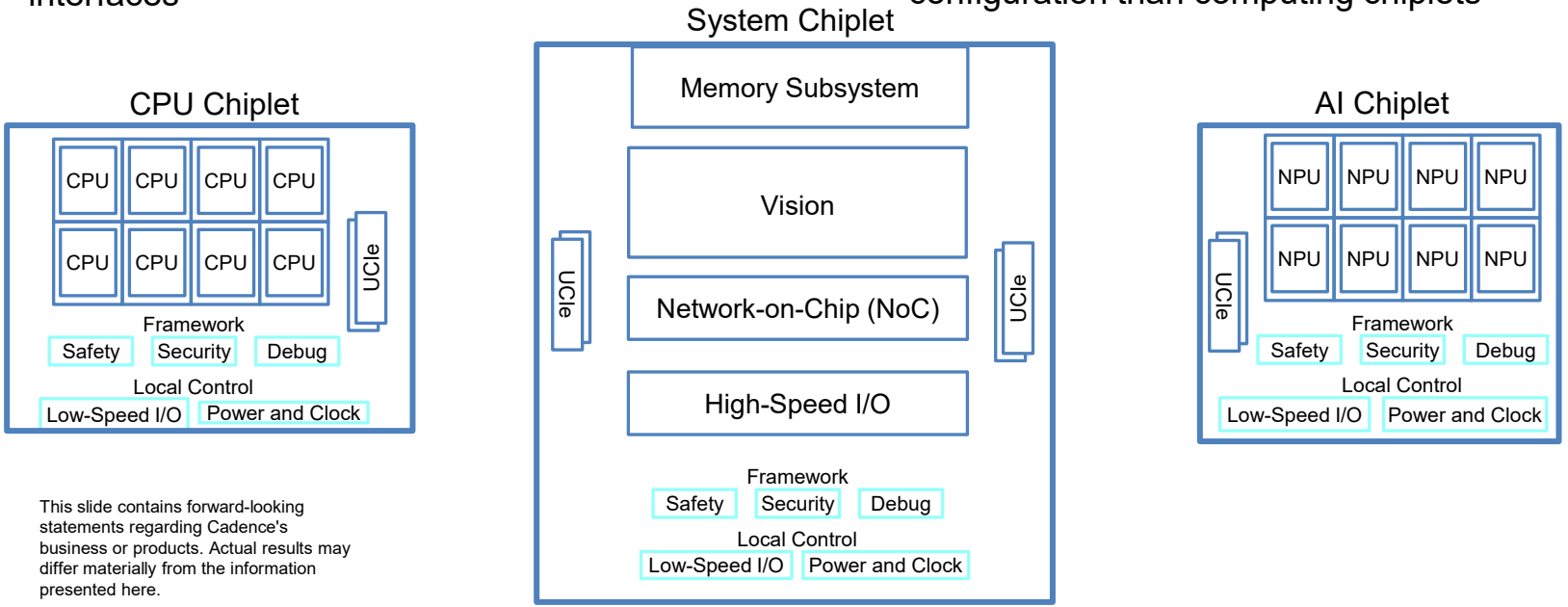
Great example for configurable and scalable systems



- Architect a set of chiplets to build a range of solutions
  - Ability to upgrade portions of the system
- Common architecture and software environment across all vehicles
  - Software verification is among the greatest challenges for automotive OEMs

Reference Platform

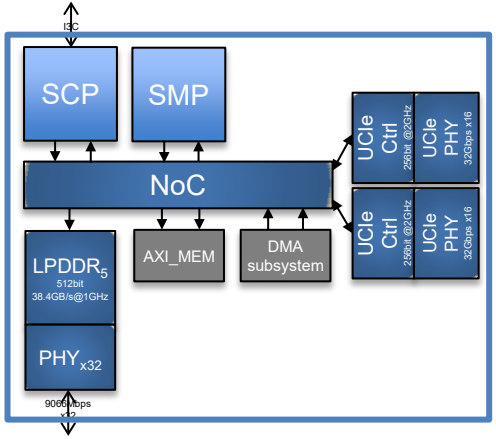
- Initial version will run at 1H'25 in emulation
- SoC-level control functionality for the security, safety, and control subsystems distributed over multiple chiplets, connected via UCIe™, I3C, and event interfaces
- Chiplet framework encapsulates the subsystem into chiplet and provides cohesive communication between the chiplets
- Base system chiplet supports a more flexible configuration than computing chiplets



This slide contains forward-looking statements regarding Cadence's business or products. Actual results may differ materially from the information presented here.

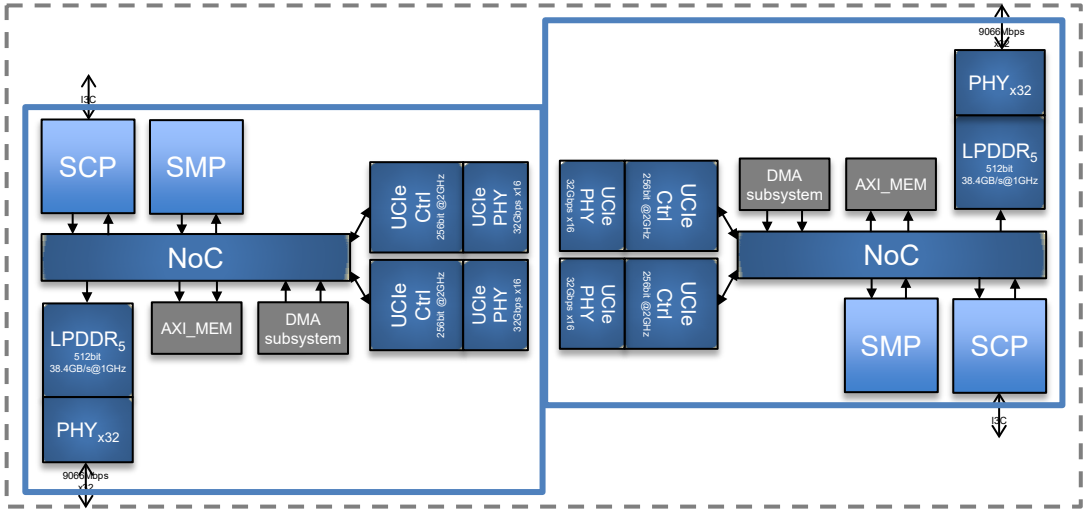
Base System Chiplet (Tapeout Completed Oct 2024)

- Advanced-node base system chiplet with system processor and LP5



Base System Chiplet

Each base system chiplet contains: UCIe™ PHY and Controller, chiplet, system control processor (SCP), safety management processor (SMP), root of trust (ROT), LPDDR5, and NoC

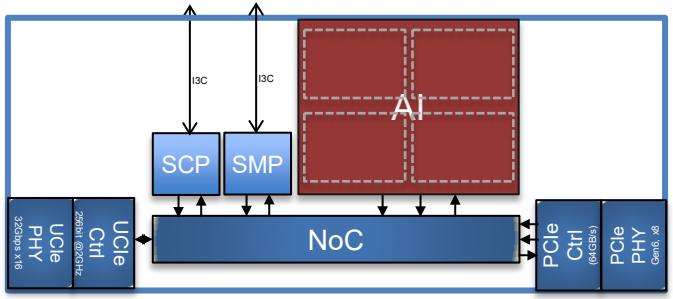


Information Classification: General

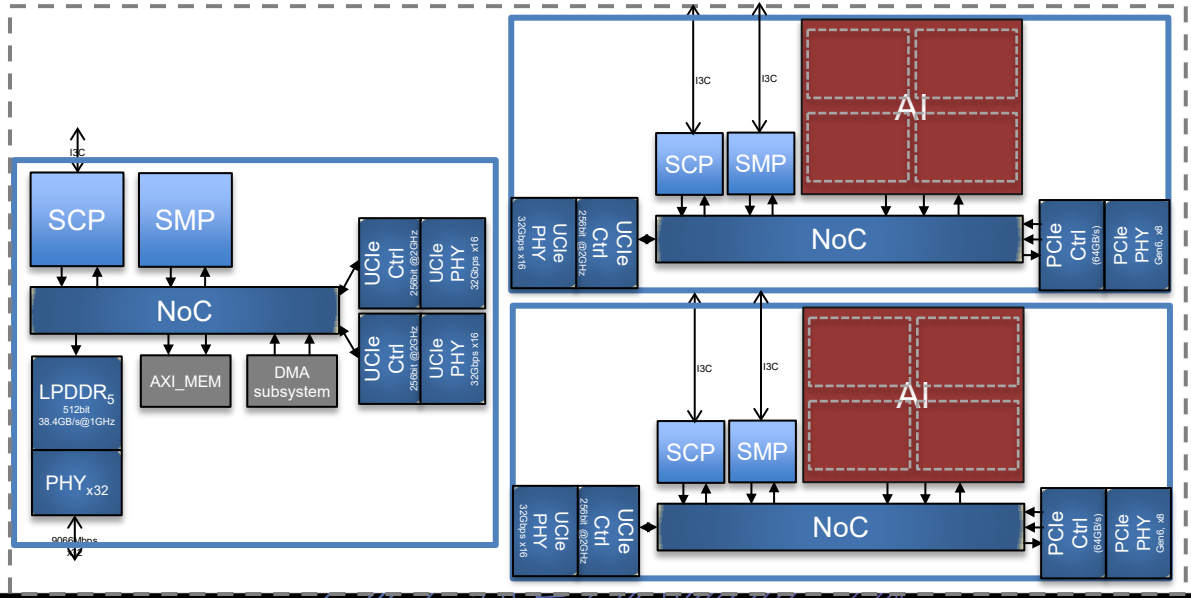
NPU Chiplet

- NPU chiplet with multi-core NPU

Each NPU chiplet contains UCIe™ PHY and Controller, system control processor (SCP), safety management processor (SMP) ROT (Root of Trust), multi-core NPU, PCIe™ PHY and controller, and NoC technology



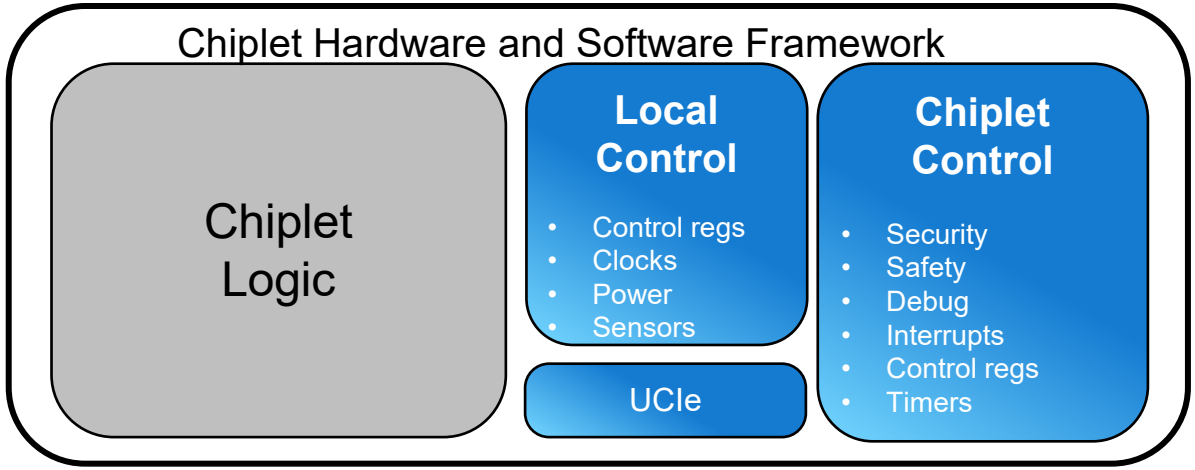
NPU Chiplet



Supporting Chiplet Architectures

Chiplet frameworks

- Supporting chip-to-chip behavior across chiplets
  - Memory interface based on UCIe™ IP
  - Security/safety/control interface based on events and I3C interfaces
- Spec-based framework to accelerate the design effort



Building out soft IP to enable the quick and correct construction of chiplets

Inter-Chip Management in System in Package

Define interoperable behavior interoperable interfaces between the chiplet

- Behavior define
  - Secure Boot (System-in-Package)
  - System Protection
  - Safety Control (Autonomous Application only)
  - System Control
  - Data Communication
  - System Synchronization
  - System Debug
- Mapping the data/event exchange into interchip interfaces
  - UCIe™ interface, (mainband and sideband)
  - Event interface
  - Signal interface

STRATEGIC ANNOUNCEMENT

SECURE-IC IS EXPECTED TO BECOME THE SECURITY ENTITY IN CADENCE DESIGN SYSTEMS

cadence x SECURE-IC THE SECURITY SCIENCE COMPANY

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1. SECURE-IC – THE EMBEDDED SECURITY ONE-STOP-SHOP
2. iNTEGRATED SECURITY SERVICES PLATFORM
   SECURYZR™
3. CYBER SECURITY EVALUATION TOOLS
   LABORYZR™
4. SECURITY CONSULTING, EVALUATION AND CERTIFICATION SUPPORT
   EXPERTYZR™
5. OUR PROMISE

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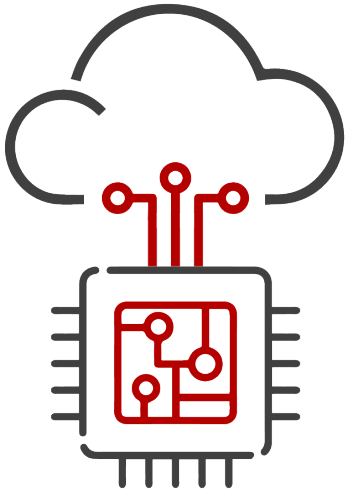
A GLOBAL LEADER IN EMBEDDED SECURITY

IoT devices being interconnected, **each and every object could be a threat for the whole network.**

Therefore, the **security of the objects or the devices with their lifecycle management is key**, and so is their data. To ensure the integrity of this data, the whole system must be secured and managed. **Trusted devices enable trusted data**.

Secure-IC partners with its clients to provide them with the best end-to-end cybersecurity solutions for embedded systems and connected objects, **from Chip to Cloud**

ONE DAY, SECURITY WILL BE WORTH MORE THAN THE DEVICES



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THE RISING LEADER IN THE SECURITY INDUSTRY

Down to **18A/2 N**

FULLY DIGITAL technology for all technology nodes and foundries

MULTI-CERTIFIABLE technologies for multiple markets

Management of security **ALL ALONG DEVICES' LIFECYCLE**

ONE-STOP-SHOP for embedded security

MATURE & WIDELY DEPLOYED solutions

10+ years

Unique & patented technologies: **ANTI-TAMPER & CYBER-PHYSICAL** attack protection

***

PQC and **AI-POWERED SECURITY**

250+ patents

350+ publications

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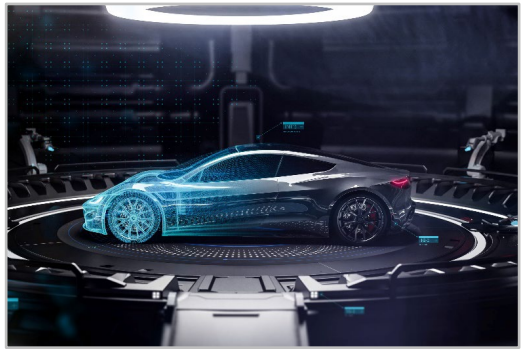
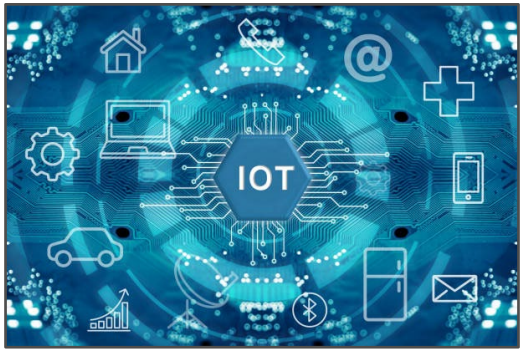
NUMEROUS MARKETS FOR EMBEDDED SECURITY

Automotive



Edge / AI / OT

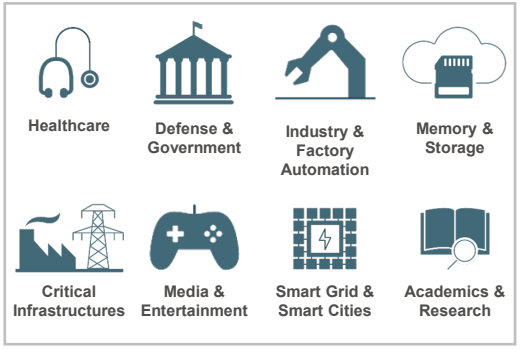
IoT



Mobile / High Security

Networking / Server

Additional Markets



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THE ROOT OF TRUST APPROACH

SUPPORT FOR ALL CHALLENGES FROM SECURITY REQUIREMENTS TO SECURITY MANAGEMENT ALONG THE LIFECYCLE OF SYSTEMS

SECURYZR™

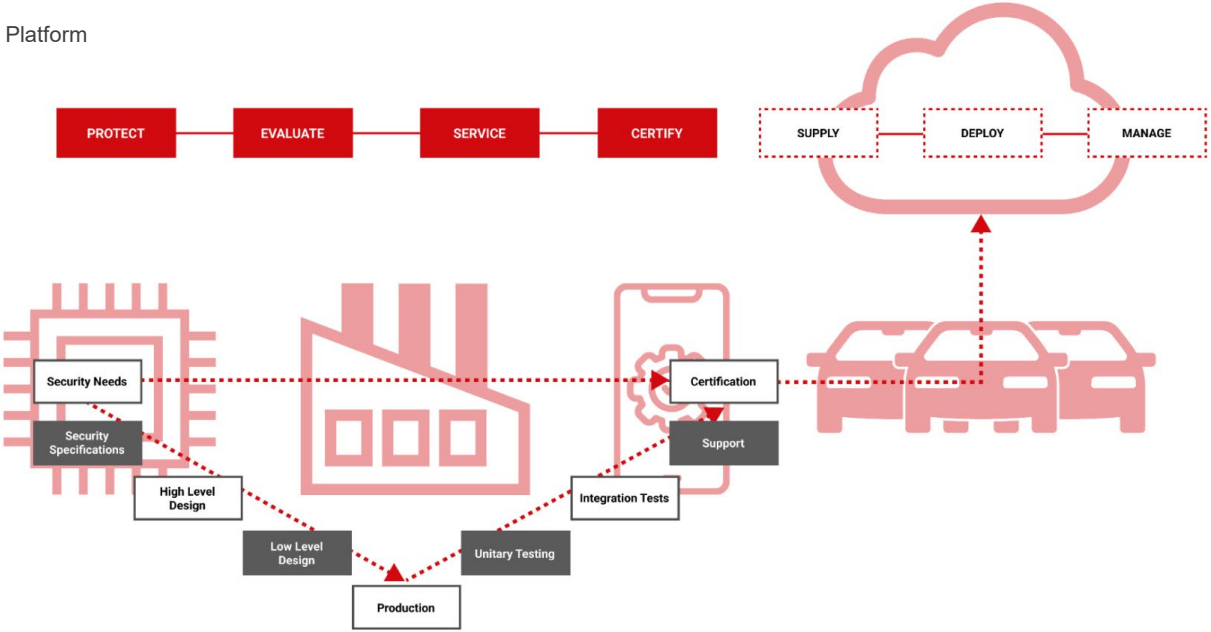
integrated Security Services Platform
Secure Hardware solutions
Secure Software solutions

LABORYZR™

End-to-end evaluation platforms for HW and SW

EXPERTYZR™

Support from experts to reach security goals
Security innovation



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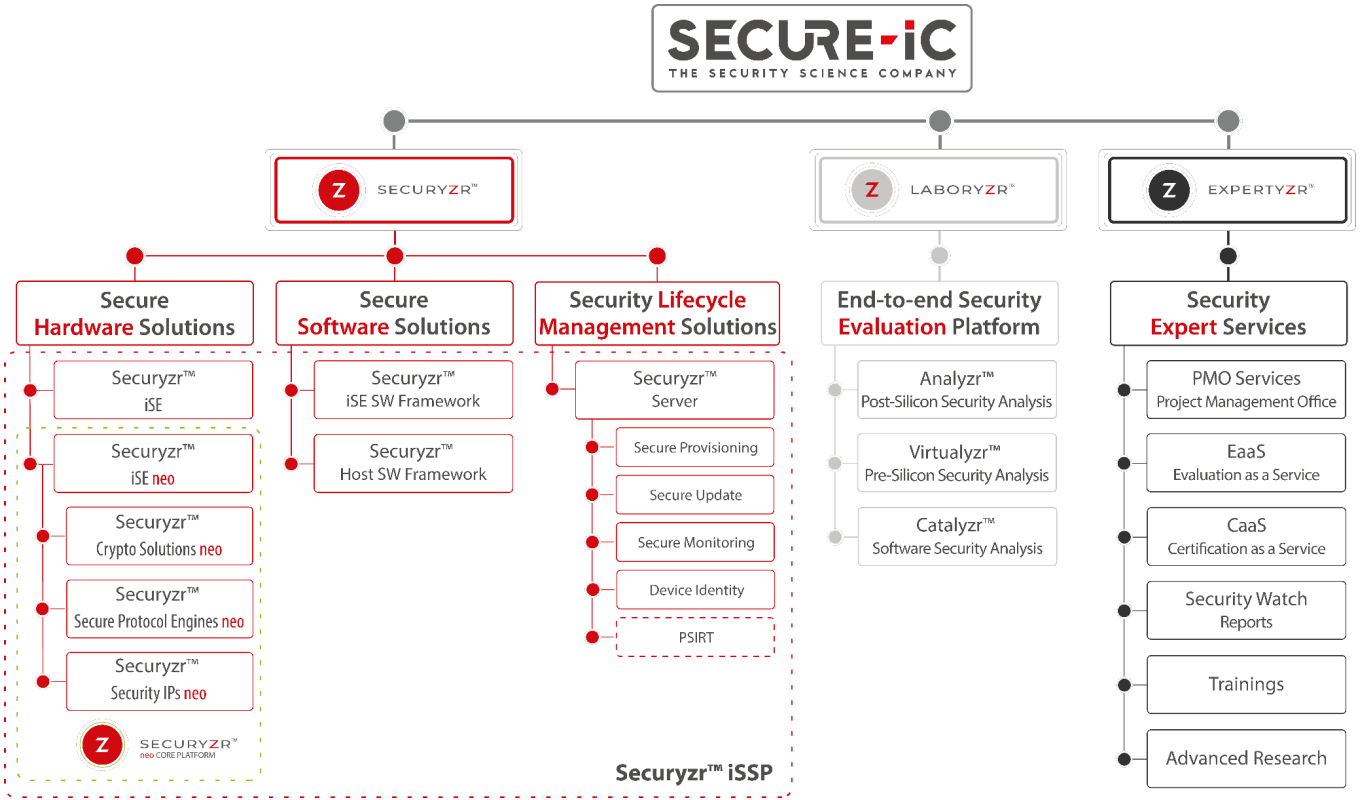
A COMPLETE SET OF END-TO-END SECURITY SOLUTIONS



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YOUR END-TO-END PARTNER FOR SECURITY ALL ALONG THE DEVICE LIFECYCLE

While globalized sourcing and manufacturing processes reduce costs, they **increase risks exposure**. Considering the complexity of value chains, the **challenge is to generate and manage trust in data**.

Secure-IC aims at answering this challenge relying on interoperability and open standards.

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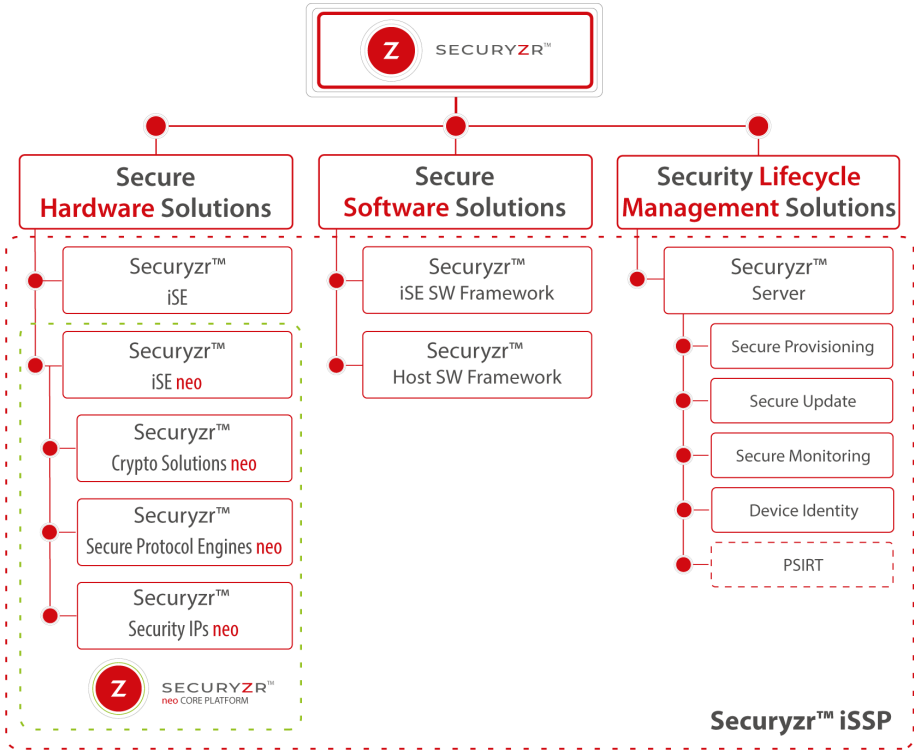
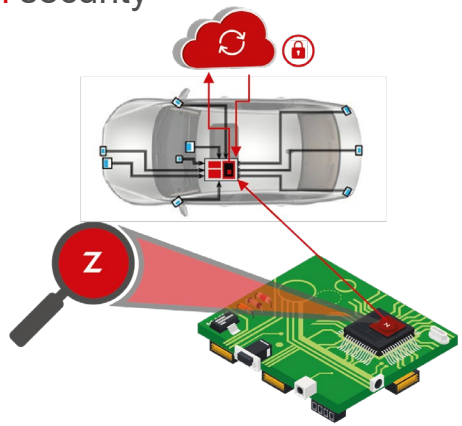
EMBEDDED SECURITY FOR ALL YOUR NEEDS



- Securyzr™ neo Core Platform
  - One core, multiple products
- **P**ost-**Q**uantum **C**ryptography (**PQC**) ready
- **ASIC** & **FPGA** compatible
- Technology node down to **2nm**
- Trustful zero-touch security server solution
- **AI** powered



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SECURYZR™ neo CORE PLATFORM

Advantages

Configurable
Reliable
Efficient
Easy Integration
Scalable
High-Performance
Lifecycle management (PSIRT)
Standards & Certifications Compliant

PQC Post-Quantum Cryptography READY

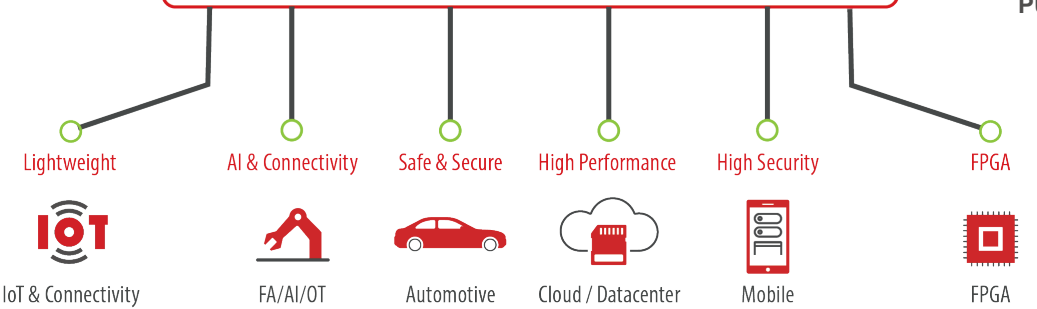
FIPS VALIDATED 140-3

ISO International Organization for Standardization

ETSI World Class Standards

SECURYZR™ neo CORE PLATFORM

ONE CORE, MULTIPLE PRODUCTS



Versatility

Per application
Off-The-Shelf Series
Pre-selected configurations
(thoroughly studied by our experts for your specific needs)
Specific options

PQC *(Post-Quantum Cryptography)*
PUF *(Physically Unclonable Function)*
TRNG *(True Random Number Generator)*
Anti-Tampering
(Active Shield or Digital Sensor)

Benefit From Secure-IC's Rich Legacy while Embracing Cutting-edge Technologies

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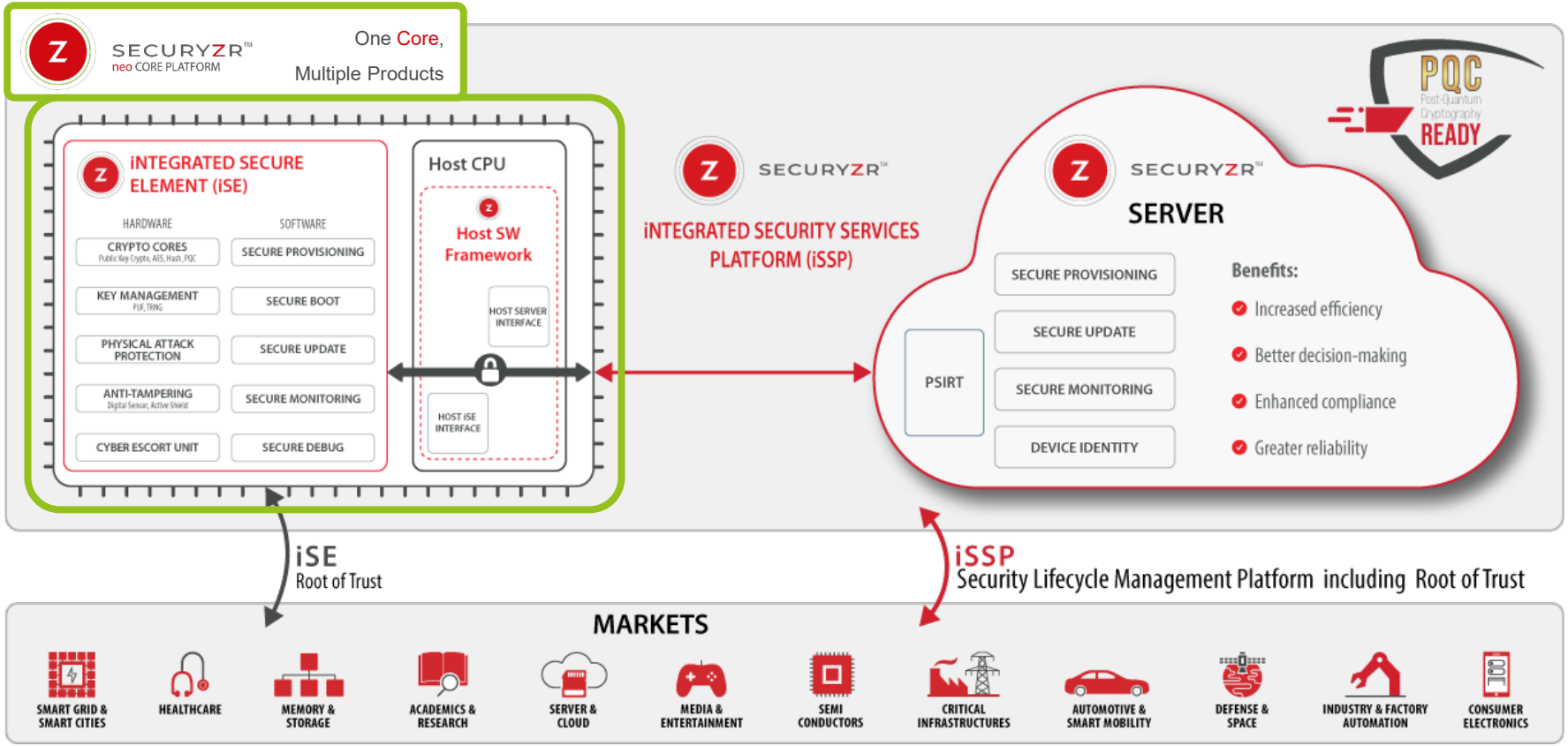
SECURYZR™ iSSP SOLUTION
MAINTAIN TRUST THROUGHOUT THE WHOLE DEVICE LIFECYCLE



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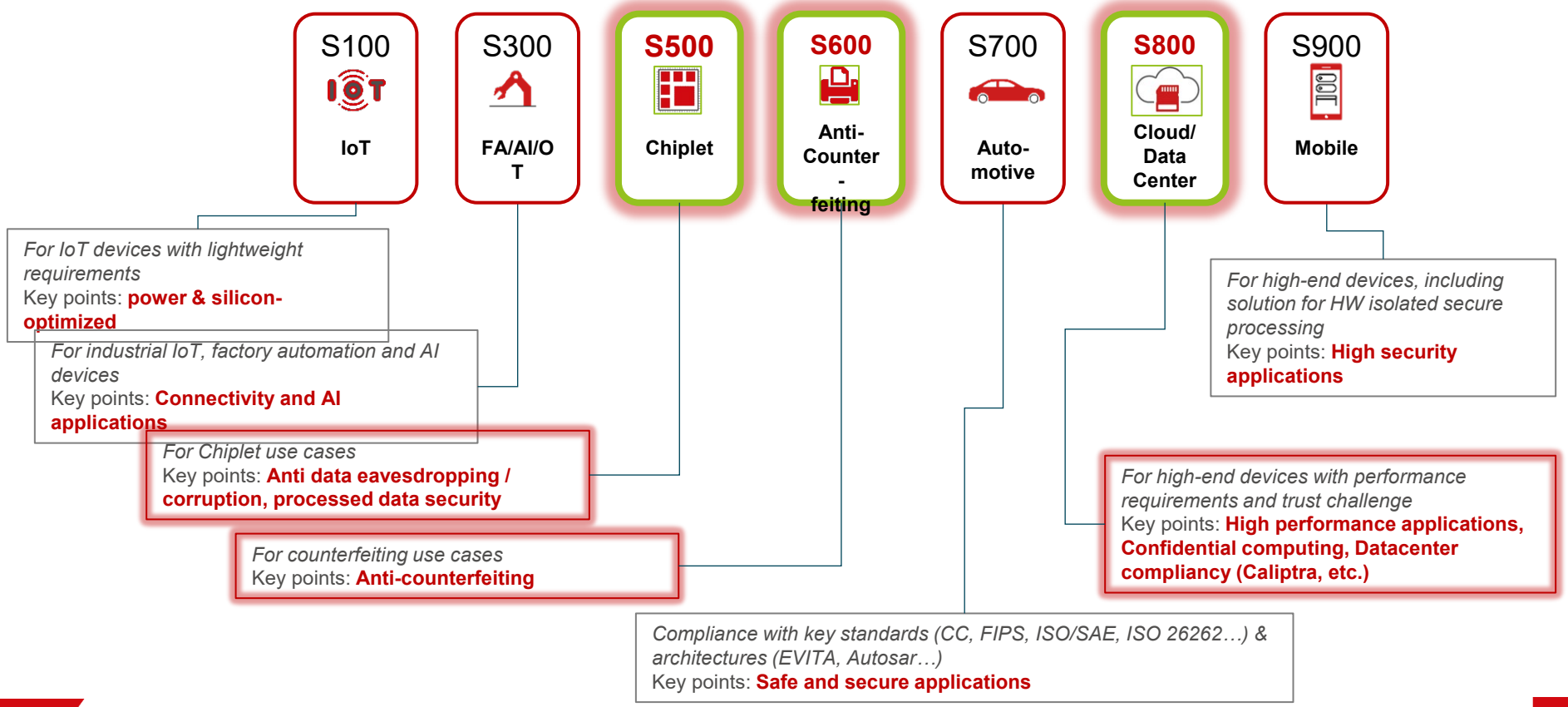
NEW SERIES



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SECURE-IC / CADENCE CHIPLET PROJECT

ADAS chiplet platform – a first successful project

cadence x SECURE-IC THE SECURITY SCIENCE COMPANY

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SECURYZR™ SERVER

SECURYZR™ neo CORE PLATFORM

PQC Post Quantum Cryptography READY

End-to-end chip to cloud security management

FLEXIBLE, EVOLUTIVE & CUSTOMIZABLE

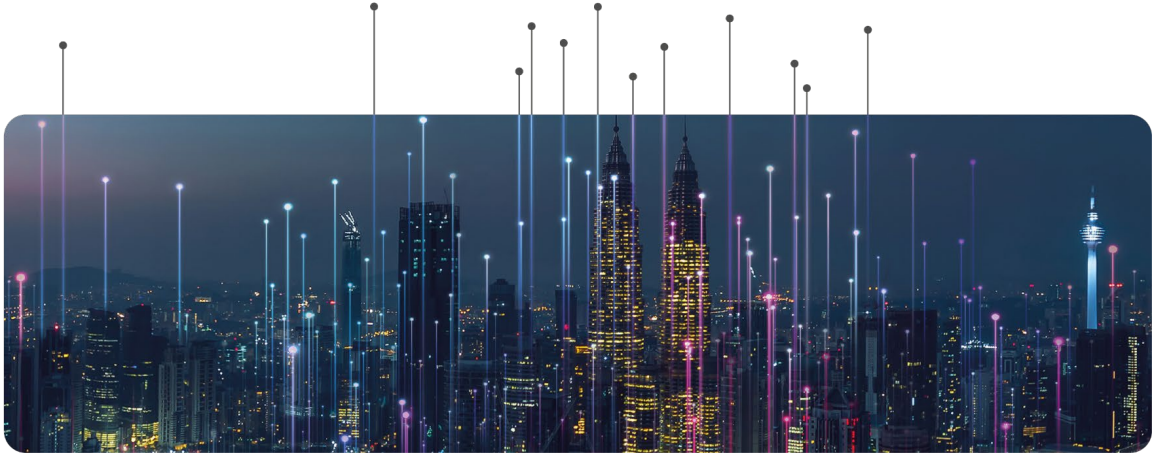
COMPATIBLE WITH TOP CLOUD PLATFORMS

SECURYZR™ SERVER

STANDARDS BASED

PERFORMANT & SCALABLE

SECURE PROVISIONING | SECURE UPDATE | SECURE MONITORING | DEVICE IDENTITY



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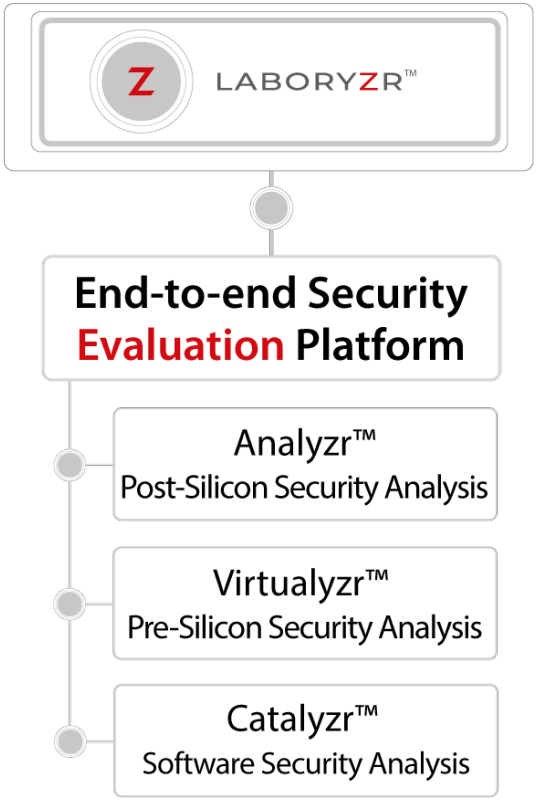
CYBERSECURITY EVALUATION TOOLS



- From **Pre-Silicon** to **Post-Silicon**
- **Side Channel** & **Fault Injection** Analysis / Attacks
- Reverse Engineering
- Hardware Trojan detection
- **Standard certifications** compliance
  - Common Criteria
  - FIPS-140
  - OSCCA
  - ISO 17825/20085
  - And more…

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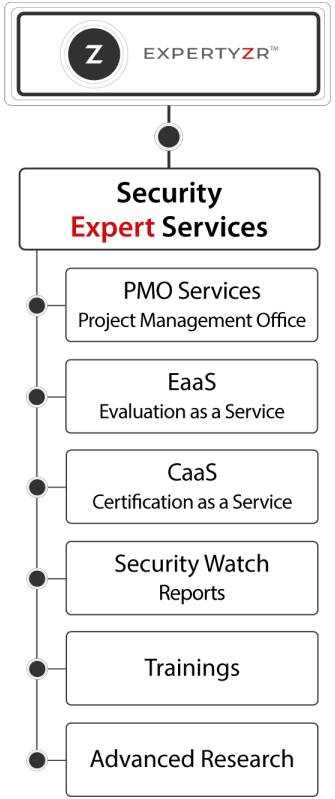
SERVICE & CERTIFY



- Security services
- Risk assessment
- **White** / **Grey** / **Black** Box analysis
- Standards & Certifications compliance check and support
- **C**yber **T**hreat **I**ntelligence
- Cybersecurity awareness
- **PSIRT**

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A COMPLETE SET OF EXPERTS' SERVICES

EXPERTYZR™

PMO SERVICES
- Project Management support to customers
- Support & Maintenance

EVALUATION AS A SERVICE (EaaS)
- Compliance with standard certification level
- Pre-silicon-Post silicon-Software evaluation
- Software code or real device evaluated Pre-Quotation & tailored Design for Security

CERTIFICATION AS A SERVICE (CaaS)
- A step-by-step guidance in the certification process from the roots to certification (CC, FIPS 140, ISO, CSPN)

EXPERTYZR™

SECURITY WATCH
- **PSIRT** (Product Security Incident Response Team) service
- State-of-the-art synthesis on major security topics and trends
- Independent audit of published attacks and practical feasibility report
- Security trend newsletter

TRAININGS
- Full catalog of theoretical and practical trainings on Embedded Cyber Security

ADVANCED RESEARCH
- Compliance with standard certification level
- Pre-silicon-Post silicon-Software evaluation
- Software code or real device evaluated Pre-Quotation & tailored Design for Security

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THE SECURITY SCIENCE FACTORY
THOUGHT LEADERSHIP

- **SCIENTIFIC WORK AND PUBLICATIONS**
  - More than 350 published papers
  - 250+ patents
- **SECURITY THOUGHT LEADERSHIP**
  - 40+ presentations per year in Semiconductor and Embedded security events

- **STANDARDIZATION**
  - Equipment for non-invasive attacks: ISO/IEC 20085
  - Physically Unclonable Functions: ISO/IEC 20897
  - White-Box Cryptography: SC27/WG3 N1367
  - Connected Car Cybersecurity: ISO/SAE 21434
  - Autonomous Vehicle Working Group 3 (AVWG 3) - Cyber Security
  - Information security, cybersecurity and privacy protection: ISO/IEC CD TR 5891 - Hardware monitoring technology for hardware security assessment
  - Side-channel leakage of cryptographic implementations assessment: ISO/IEC 17825

ISO

Standards Development Organisation

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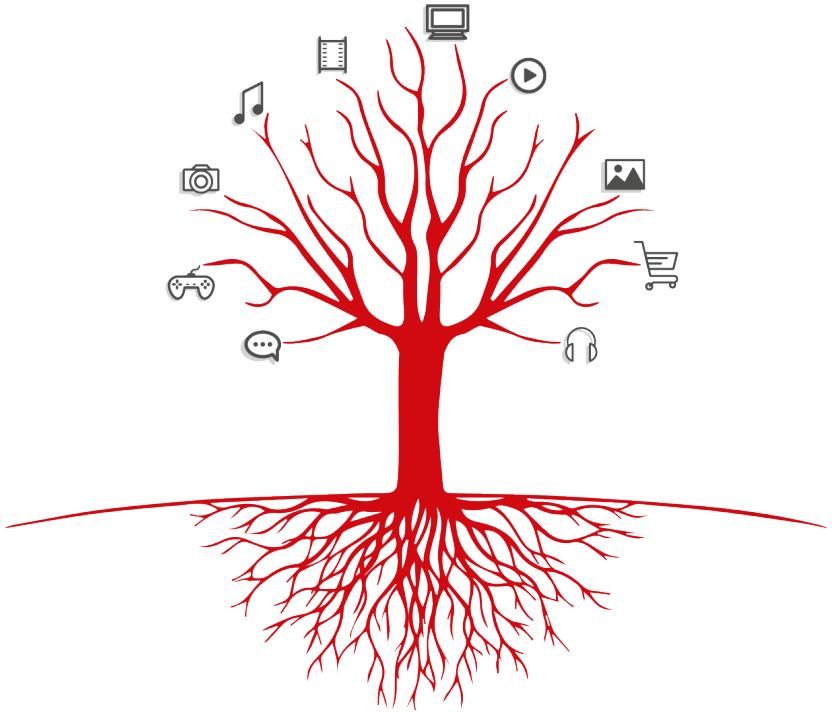
OUR PROMISE
CREATE TRUST FROM CHIP-TO-CLOUD

- Secure-IC is a trust enabler, thanks to its unique positioning as a **one-stop-shop security partner**
- Protection from **Edge Device chips to Cloud**, along their lifecycle
- **PQC** is the next revolution and Secure-IC is a pioneer in the field
- **Root of Trust**, security in depth by design



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SECURE-IC
THE SECURITY SCIENCE COMPANY

Thank you!

QUESTIONS?

Sam Wong

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