Welcome to

30th ANNIVERSARY

DESIGNCON® 2025

WHERE THE CHIP MEETS THE BOARD

Conference

January 28–30, 2025

Santa Clara Convention Center

Expo

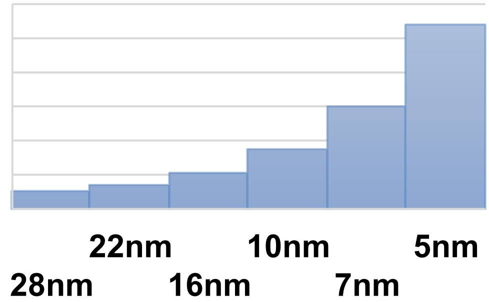
January 29–30, 2025

The Role of EDA as Chips Transform Into 3D Systems

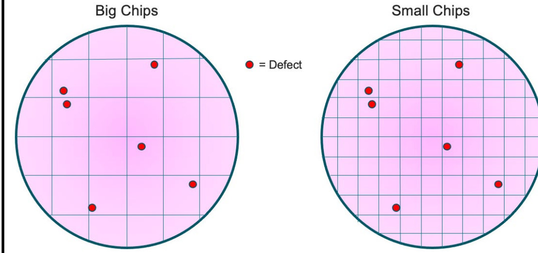
John Park, Cadence

For ASIC Designers, Simply Following Moore's Law Alone Is No Longer the Best Technical and Economical Path Forward

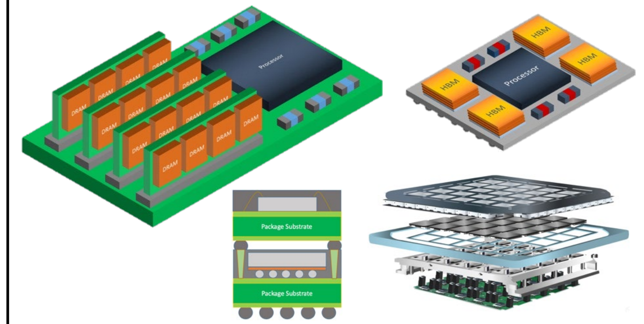
Cost



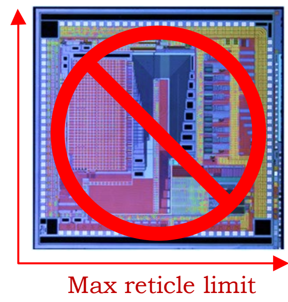
Yield



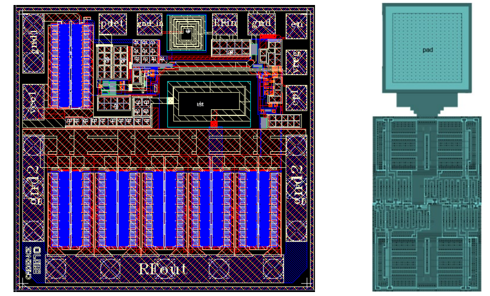
Memory Bandwidth



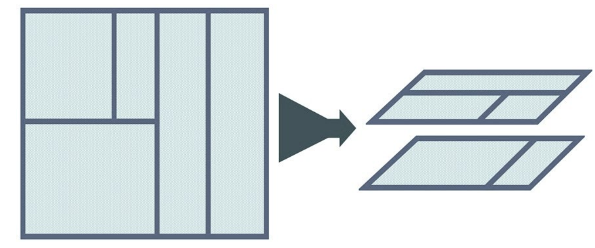
Size



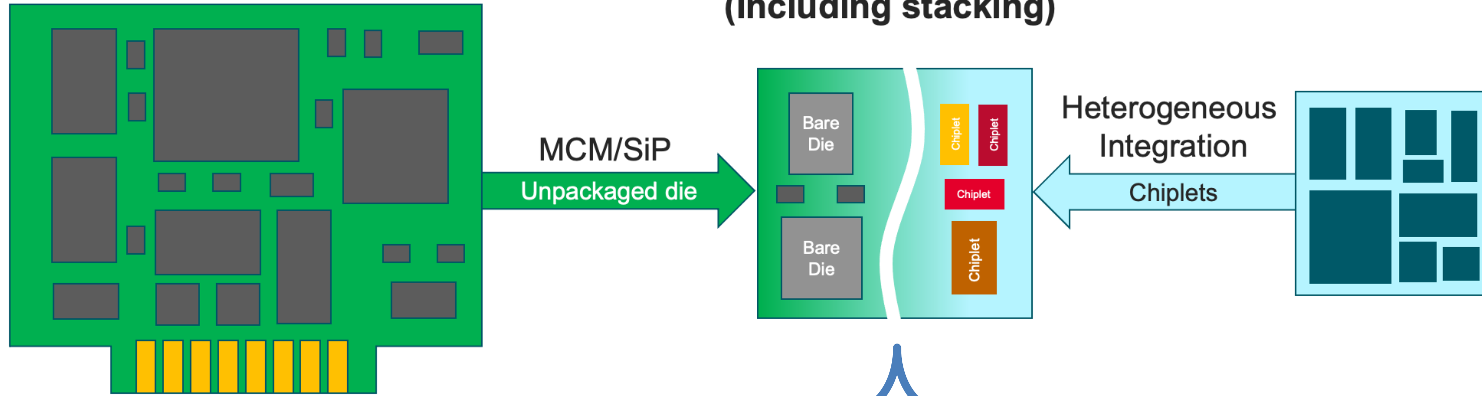
Analog/RF and I/O

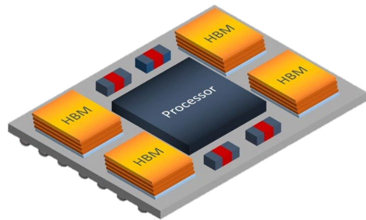


Form Factor and Modularization

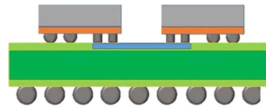


Technology Breakthroughs in Semiconductor Packaging is Key to Transforming Chips Into 3D Systems

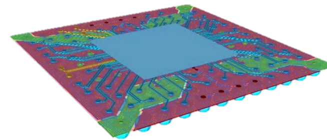




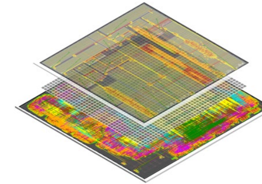
Silicon/Glass/RDL Interposers



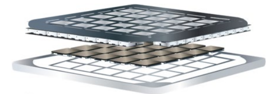
Interconnect Bridges



Ultra-High-Density RDL



Bumpless Chip-on-Wafer Stacking

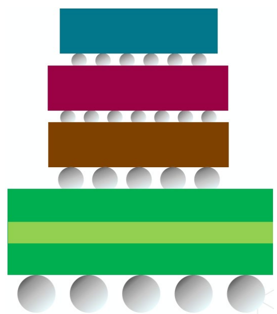


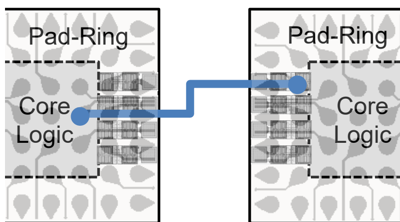
Wafer-On-Wafer Stacking

3D Packaging vs Chip/Wafer Stacking (3DHI)

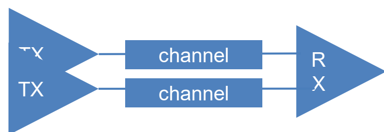
3D Packaging

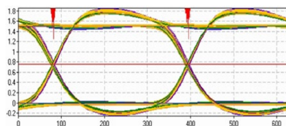
- Solder-based connections (35-150um)
- Dies designed independently
  - Black-box modeling
- I/O buffer-to-buffer signaling





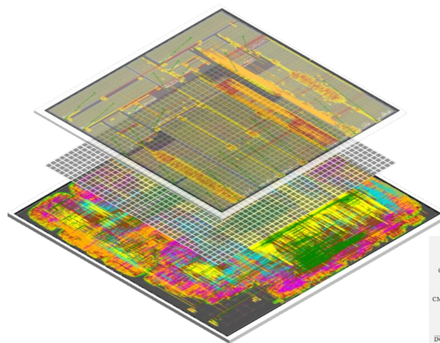
I/O buffer to I/O buffer
(BoW, UCIe, AMBA CHI, UMI, etc.)

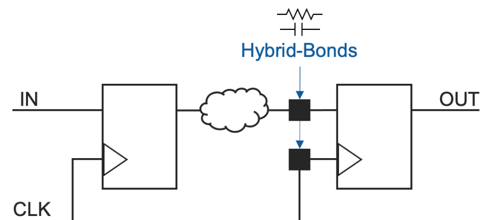




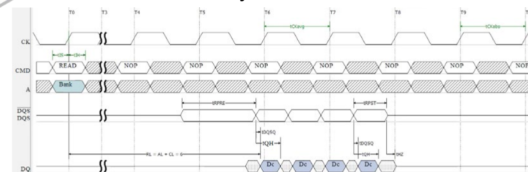
Chip/Wafer 3D Stacking

- Solder-free connections (<10um)
- Single RTL partitioned at implementation
  - Full detail of IC required for layout
- DBI, hybrid-bond, cu-to-cu, and direct connection





Interconnect through hybrid bond



The Wild West of Semiconductor Packaging

100s of ways to package devices

Leadframe	Single Substrate (Routable)	Multi-Tech/Hybrid Substrates	Multi-Substrate (Interposers/ 2.5D-IC)	Substrate-less (WLCSP/ FOWLP	Wafer/Chip Stacking (3D-IC)

DESIGNCON® 2025
WHERE THE CHIP MEETS THE BOARD
Information Classification: General

JAN. 28–30, 2025

#DesignCon

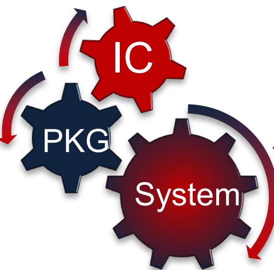
informa markets

Convergence of Electrical/Optical/Mechanical 3D Systems, and Chips Leads to Extremely Complex Design Flows

OSATs (SWaP)

Board design impact on packaging

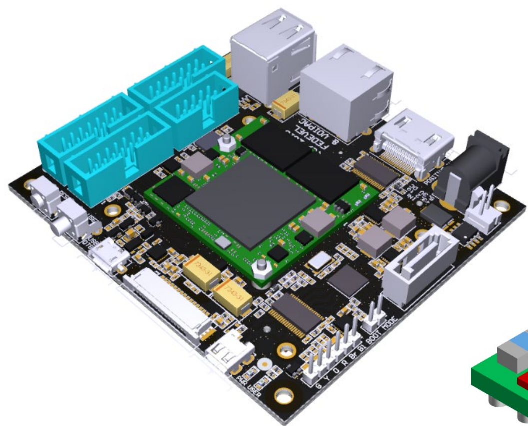
1980-2010

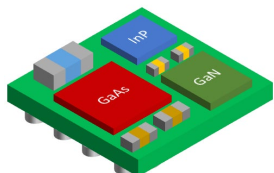


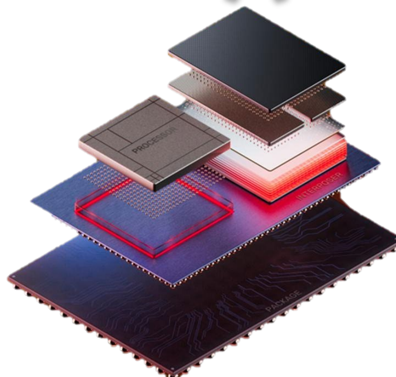
Foundries (PPA)

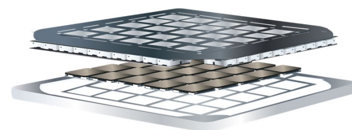
IC design impact on packaging

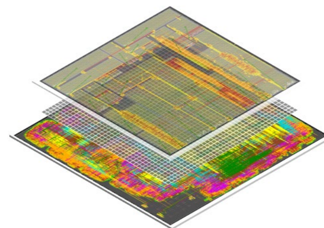
2011-Now

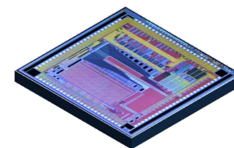












PCB Layout Flow
System-Level Analysis

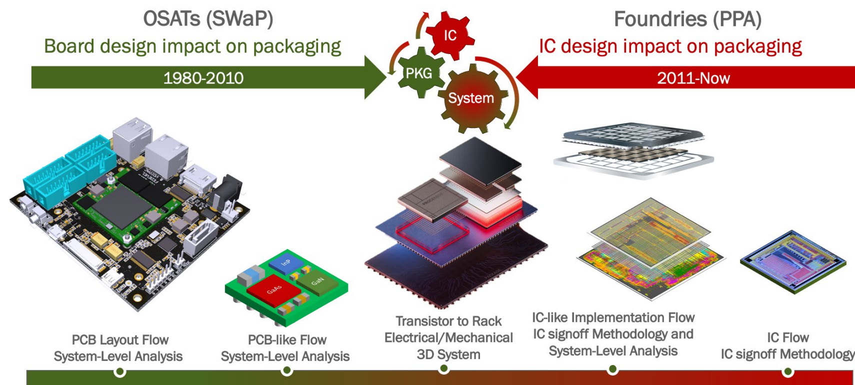
PCB-Like Flow
System-Level Analysis

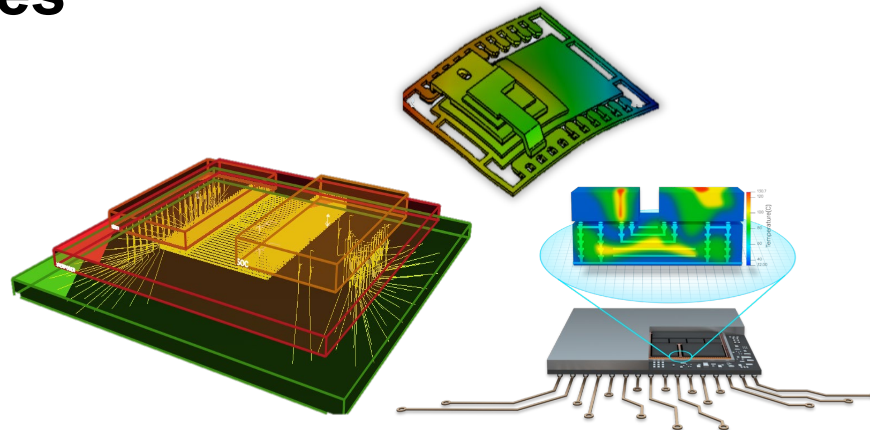
Transistor-to-Rack
Electrical/Mechanical
3D System

IC-Like Implementation Flow
IC Signoff Methodology and
System-Level Analysis

IC Flow
IC Signoff Methodology

Design and Analysis Challenges





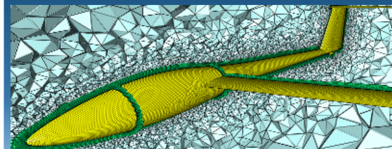
Complex Design Flows

- Convergence of systems and ICs driving an explosion in the number of design tools and leads to complex design flows
  - Mechanical tools will be next to come
- Co-design/co-analysis across die/chiplet/package
- Support for existing and emerging 3D-IC standards
- Layout stage too late for electrical and thermal analysis
- All tools need to be three-dimensional system-aware
  - Complex 3D floorplans

Implementation and Signoff

- Lack of design manufacturing and assembly data
  - Assembly design kits (ADK) are lacking
  - Single source of truth
- Laminate design vs. silicon design
  - Advanced IC-style design rules
  - SystemLVS
- Mechanical engineering tasks (warpage, cold plates, etc.)
- D2D and D2S routing bottlenecks

Digital/Analog/RFIC, SiP/MCM, PCB, and System Analysis

IC Design	Simulation	SiP/MCM and PCB	Systems Analysis
Innovus™, Virtuoso®, and Microwave Office®	**Spectre®, Legato™, and Xcelium™**	**Allegro® X, OrCAD® PSpice®, InspectAR, and Pulse**	**Clarity™, Celsius™, EMX® Fidelity™, Voltus™, and Sigrity™**
Advanced node/ML automation	Digital logic verification	High-speed PCB	2.5 and 3D electromagnetics
Digital, analog, RF, and photonics	Reliability	Advanced IC packaging	Electrothermal
MMIC	RF and AMS simulation	Augmented reality and ML/AI	Computational Fluid Dynamics
			

Cadence.AI – Cadence® Joint Enterprise Data and AI (JedAI) Platform

Generative AI Applications

Digital Design	Analog/Custom Design	Debug and Verification	PCB Design	Multiphysics Optimization

Ecosystem Collaboration and Partnerships

EDA Optimized Customer and Cadenced Managed Cloud-Based Solutions

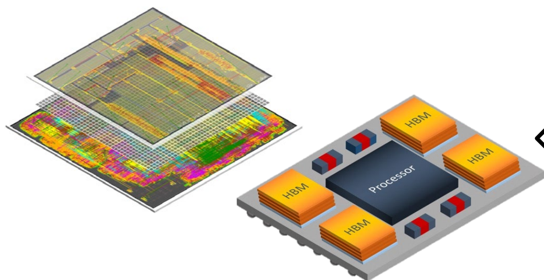
Integrity™ 3D-IC Platform

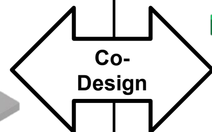
Integrity System Planner
(Top-level planning, optimization, and early-stage analysis)

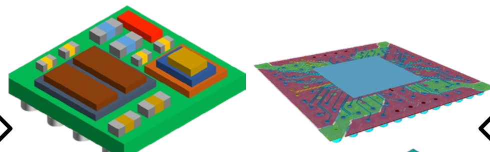
Virtuoso®/AWR®
(Analog/RF/Photonics)

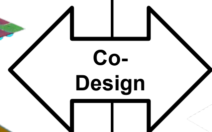
Integrity 3D-IC

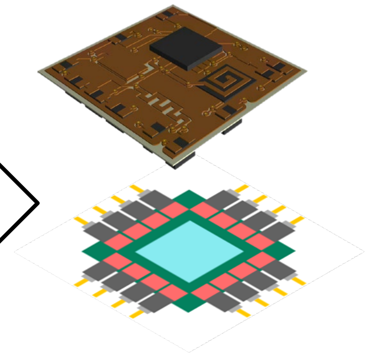
Allegro® X APD











Allegro X (Integrity Option)

Allegro X

Sigrity™ X, Clarity™, Celsius™, Voltus™, and Pegasus™
(EM-IR, 3D-EM, signal-integrity, system power/thermal, DRC/LVS, and SystemLVS signoff)

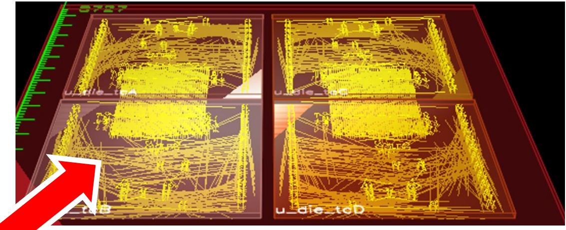
Digital IC Designer
Primarily LINUX OS
Chip-on-wafer and wafer-on-wafer
Based on Innovus™ 3D-IC
Die/chiplet detailed editing level

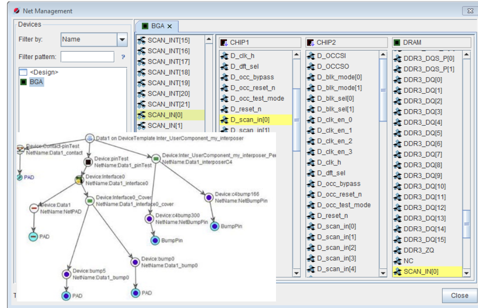
Package Substrate Designer
Primarily MS Windows OS
Multi-die, multi-chiplet substrate layout
Die abstract editing level
3D-EM, signal integrity, and system power

RF-IC Designer
Primarily LINUX OS
Targets RF module design
Integrated circuit simulation
Electromagnetics extraction

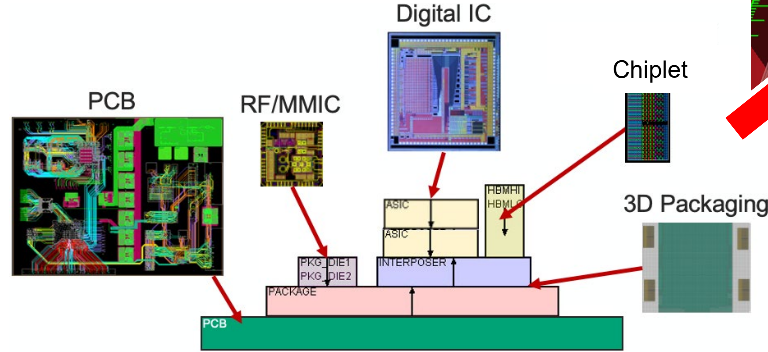
Integrity System Planner

3D system-level aggregation and optimization

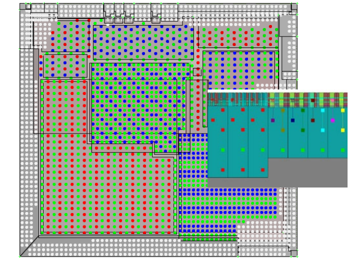




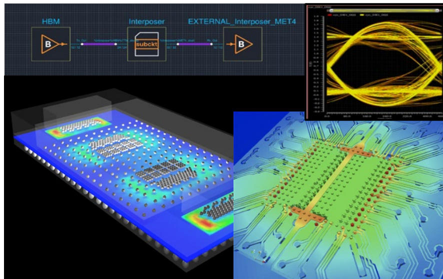
Chip(let)-chip(let)-package-board signal-mapping



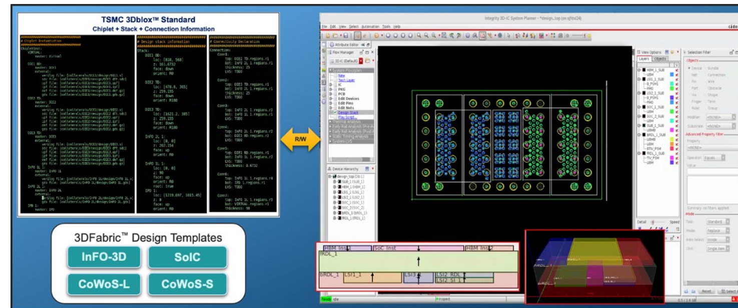
Hierarchical Planning and Optimization of System-Level Design and Connectivity



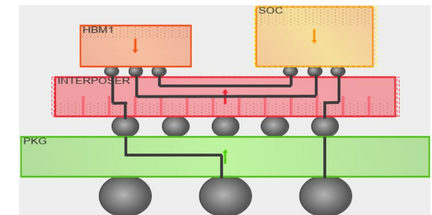
Advanced bump/TSV/TDV planning



Early-Stage Power/Thermal/SI Analysis



3Dblox™ & 3DCODE Support



SystemLVS (Rule-Deck-Free)

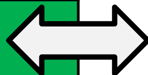
Allegro X Multi-Chiplet 3D Packaging Sub-Flow

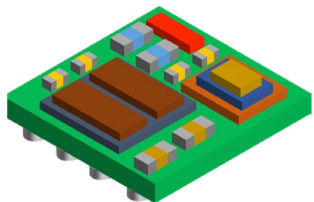
Integrity™ System Planner
(Planning, optimization and early-stage analysis)

PVS/Pegasus™
(Physical Verification)

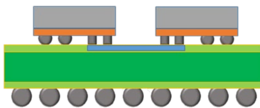
Allegro® X Package Designer

Silicon Layout Option

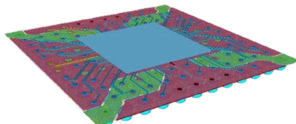




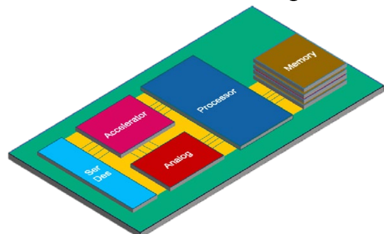
SiP/MCM



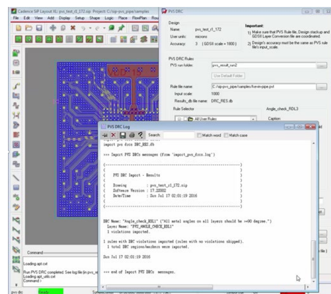
Interconnect Bridge



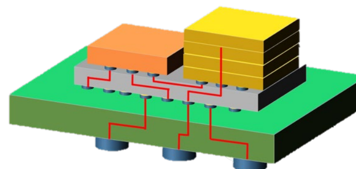
FOWLP



RDL Interposer



Signoff DRC



SystemLVS

Sigrity™ X, Clarity™, Celsius™, and Voltus™
(3D-EM, Electrical and Thermal Signoff)

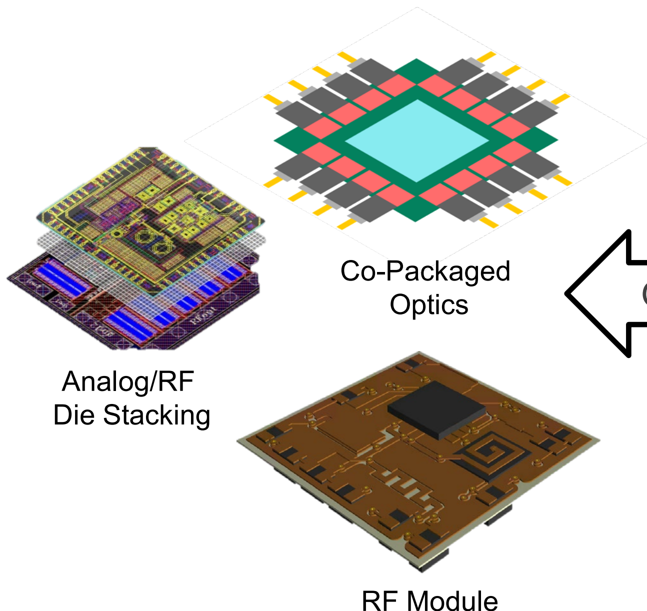
- Techfile-driven correct-by-construction layout
- Supports OSAT and foundry-based packaging technologies
- Flexible connectivity creation, including layout-driven design
- Automated library development
- Seamless 3D-EM and thermal modeling integration
- In-design electrical analysis, DFA, and DFM
- Co-design capabilities with Innovus™ and Virtuoso®

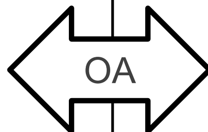
Analog/RF/Photonics Sub-Flow

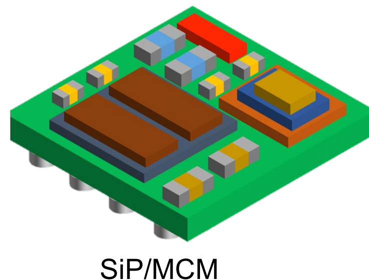
Virtuoso®
(Analog/RF IC design platform)

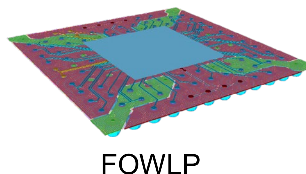
Integrity™ System Planner

Allegro® X Package Designer









Sigrity™ X, Clarity™, Celsius™, and Voltus™
(3D-EM, electrical and thermal signoff)

- Single hierarchical schematic for complete system co-design
- Multi-tech enables multi-PDK concurrent design
- Edit-in-Concert advanced cross-domain co-design
- Seamless integration of on-chip and off-chip EM
- Modeling of die to package cross-coupling effects
- Automated layout parasitic back annotation flow
- Unified library and SystemLVS

Cadence Capabilities Enabling Electronic Product Realization

EDA Design Tools

- Digital IC
- Analog/RF IC
- Advanced Packaging
- 3D-IC
- PCB
- MMIC
- Thermal
- Power
- Signal Integrity
- 3D Electromagnetics
- CFD
- Functional Verification
- STA
- Physical Verification
- System Planning
- Reliability
- Data Management
- 3D Mechanical
- …

Reference Design Flows

- 3DHI
- RF-IC
- Digital ASIC
- System analysis
- Partner software overlays

Design IP/Chiplets

- D2D (UCIe)
- DIP
- TIP
- Security
- …

Design Services

- ITAR Compliant
- Digital ASIC
- 3DHI
- RF module
- …

Government Programs

- DARPA CHIPS
- RAMP/RAMP-C
- ERI
- SHIP
- NGMM
- NAPMP
- …

Cloud

- On-Prem
- Hybrid
- Secure Gov
- …

Emulation

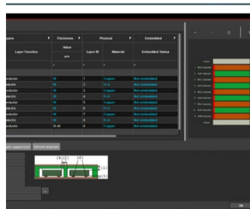
- ASIC
- FPGA
- Digital Twinning
- …

Assembly Design Kits

- PDK for 3DHI
- ADK Automation
- ADK Collaboration
- All stages of design

Cadence Assembly Design Kit (ADK)

TechFiles



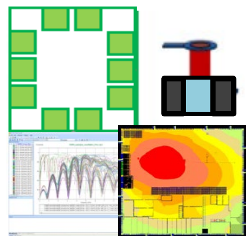
Layer stack-up
- Material
- Properties
- Thickness

Physical/Electrical layout constraints
- Line and space
- Differential signaling

Customized in-design DRCs
- RAVEL

Design templates

Design Libraries

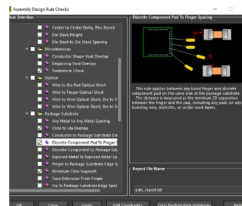


Footprints and Power/Thermal models
- Chiplets
- Discrete
- BGA/LGA/Interposer
- Via structures
- D2D routing topologies

STEP Models

Library compare

Assembly Rules

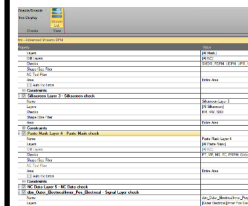


Device placement constraints based on assembly pick and place equipment
- Device to device spacing
- Device to obstacle
- Device to edge
- Max stack height

Compliance Kits

Electrical spec validation of chip(let)-to-chip(let) interfaces
- Interconnect library
- I/O libraries
- Eye masks
- Jitter tolerance
- Insertion/return loss

Manufacturing Rules



Board/substrate manufacturing process
- Substrate checks
- Soldermask checks
- Soldering issues
- Silkscreen checks
- Tech file compare

Rule Decks

Foundry/ semiconductor manufacturing process
- DRC
- LVS
- SystemLVS
- Metal fill

Benefits of an Assembly Design Kit

Benefits of an ADK
Bounds the packaging challenge for high-volume design manufacturing
Creates a more seamless interaction between end-customer and OSAT/Foundry
Provide collateral necessary to run all tools in supported flows, enabling consistency across users
Single source of truth for multi-chip packaging
Organize data so that users don't have to guess at tool setups
Prevent manual entry/error by users of critical foundry data (line spacing, vias, etc.)
Supports private and public repositories
Creates self-contained workspaces and manages versions and ECOs
An ADK is specific to a particular CAD tool/flow

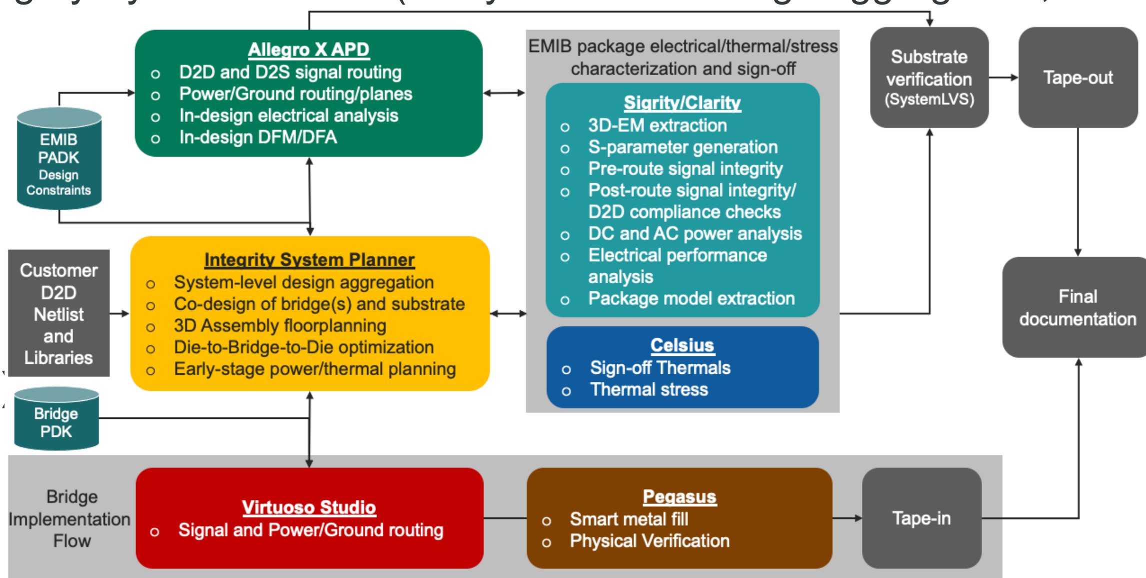
What an ADK is NOT
Cadence helps companies build ADKs, we don't provide ADKs
ADKs are not a design/layout service
For single-use case
There is no industry standard for an ADK

Cadence Has Tools/Flows to Support All Multi-Die, Multi-Chiplet 3D-HI Packaging

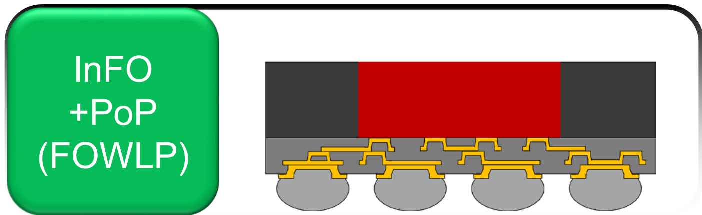
Package Type	Integrity™ 3D-IC Platform	Virtuoso® Studio (VMT)	Allegro® X Silicon Layout Option	PVS/ Pegasus™ (DRC/LVS)	Sigrity™/Clarity™ (3D-EM, System Power, and SI)	Voltus™ Fi (Die-Level EMIR)	Celsius™ (Thermal)	EMX® (Die-Level EM)
Wirebond BGA			✓		✓		✓	
FC BGA/LGA			✓		✓		✓	
LTCC			✓		✓		✓	
FOWLP			✓	✓	✓		✓	
Interconnect Bridges	✓[B]	✓[B]	✓[S]		✓[S]		✓	
RDL Interposer			✓	✓	✓		✓	
Silicon Interposer	✓	✓		✓	✓	✓	✓	✓
Glass Interposer			✓	✓	✓		✓	
Bumped Stack	✓	✓	✓	✓	✓	✓	✓	✓
Bumpless Stack	✓	✓		✓		✓	✓	✓

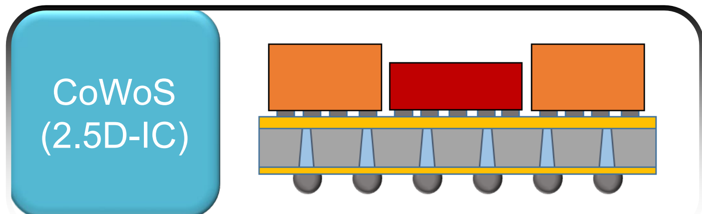
Cadence and Intel Foundry Collaborate to Enable Multi-Chip(let) Design with EMIB Packaging Technology

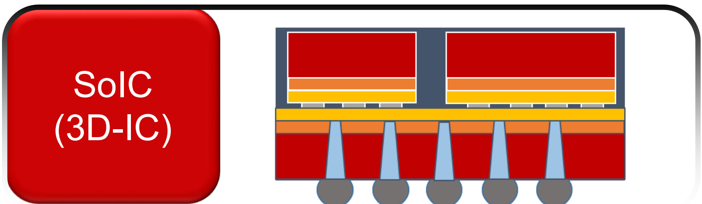
- Joint effort has resulted in an advanced packaging flow:
  - Cadence's Allegro® X APD (for placement, signal/power/ground routing, in-design electrical analysis, DFM/DFA and final manufacturing output)
  - Integrity™ 3D-IC Platform and Integrity System Planner (for system-level design aggregation, planning and optimization)
  - Sigrity™ and Clarity™ solvers for two-parameter generation, early-stage and signoff signal integrity, DC/AC power analysis, and packaging model extraction)
  - Celsius™ solvers (for early-stage and signoff thermal signoff/stress)
  - Virtuoso® Studio (for signal/power/ground routing of EMIB bridges)

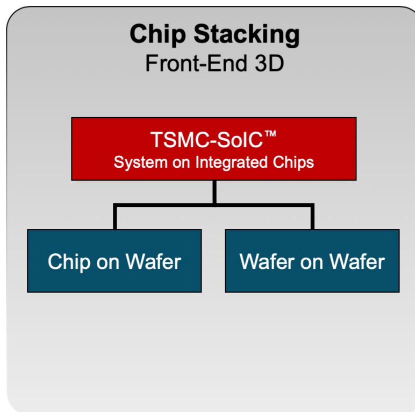


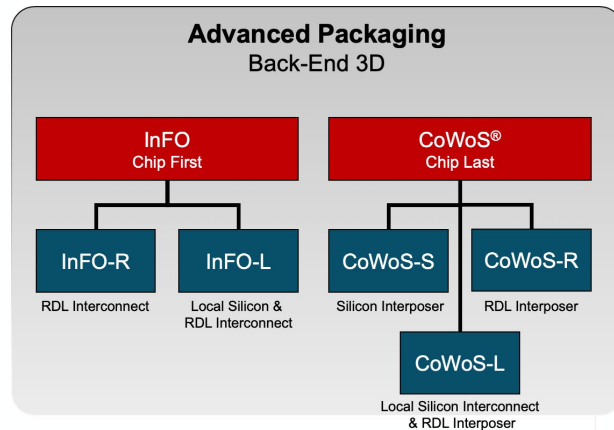
Reference Flows for TSMC 3DFabric™ Wafer-Level System Integration Technologies











Cadence Tools Currently Certified for TSMC 3DFabric™ Flows

Function	Tools
Top-Level Management	Integrity™ System Planner
Physical Design	Innovus™
	Virtuoso®
	Allegro® X
Verification	Pegasus™-DRC
	Pegasus™-LVS

Function	Tools
Modeling/ Extraction	Quantus™
	Sigrity™ XtractIM™
	Clarity™
Analysis	Tempus™
	Voltus™
	Sigrity SystemSI
	Sigrity PowerSI®
	Celsius™

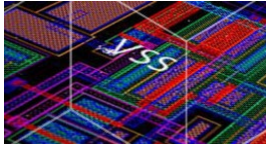
Cadence Transforms Chip Through Systems

Design Solutions

partnership

Data Center
Digital Twin

Chip



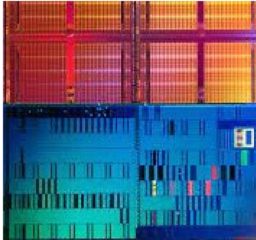
Package

Board

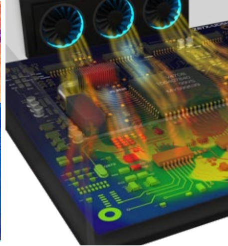
Systems

Multiphysics Analysis

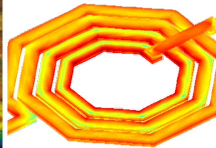
IC EM-IR



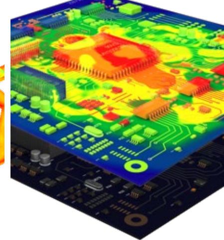
Electrothermal



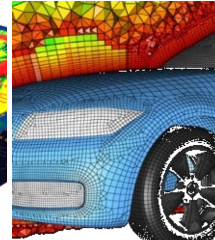
IC 3D-EM Solver

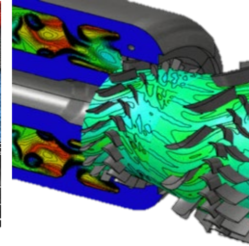


Signal Integrity System Power



CFD, Meshing





Enterprise Data Platform (Cadence® JedAI)

Thank you!

QUESTIONS?

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