Welcome to

Conference
January 28–30, 2025
Santa Clara Convention Center

Expo
January 29–30, 2025

Accelerate Silicon Interposer Development with Integrated Design and Analysis – A Cadence Exclusive

Pedro El Awar, Cadence

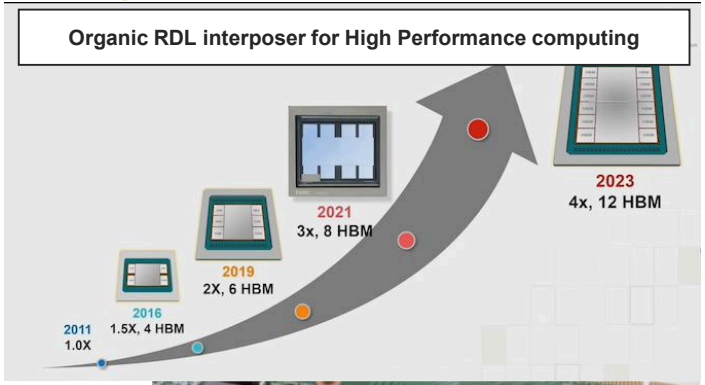
Agenda

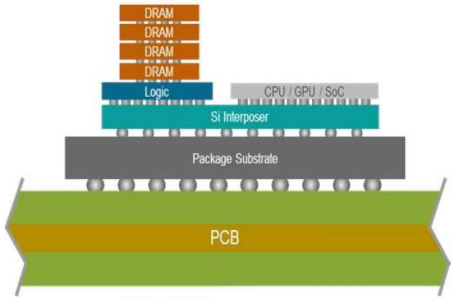
- Problem Statement: Growing Complexity – Ultra-high-end packaging technologies being pushed to their limits
- Algorithmic Selective Cutting Methodology Proposition
  - Design platforms (Allegro® X PCB, Allegro X Advanced Package Designer)
  - Simulation domain (In-design analysis, Sigrity™ SI/PI, Clarity™ 3D Solver)
- Algorithmic Selective Layout Cutting
  - What it is
  - How it benefits design and simulation
  - Benchmarks
- Intelligent Multi-Block Extraction
  - Motivation, what it is
  - How it benefits analysis
- Applications of the Intelligent Selective Cutting Methodology
  - AI-driven design synthesis with constraints
  - System-level SI post-route optimization methodology
  - PDN analysis
  - Heterogeneous system extractions
- Conclusion and Next Steps

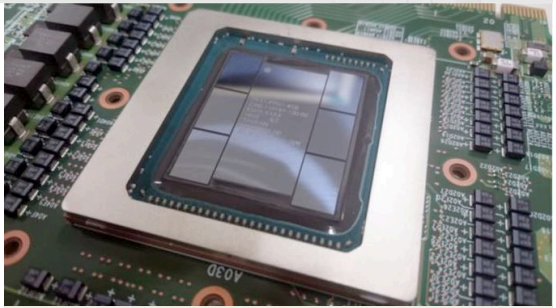
Problem Statement

Growing complexity – Ultra-high-end packaging technologies being pushed to their limits

- In recent years, high-performance computing chip designs are pushing ultra-high-end packaging technologies to their limits
- Translators and layout tools cannot scale linearly to address the growing scale of engineering designs
- Need to provide customers the ability to distribute the layout and analysis efficiently within scalable workflows
- **Parallelization**, **integration,** and **Turn-Around-Time (TAT)** are keys to success
  - Need to better integrate the layout of interposers, IC packages, and PCBs within the simulation and analysis domain (**multi-fabric analysis**)
  - More extractions needed and earlier in the design cycle







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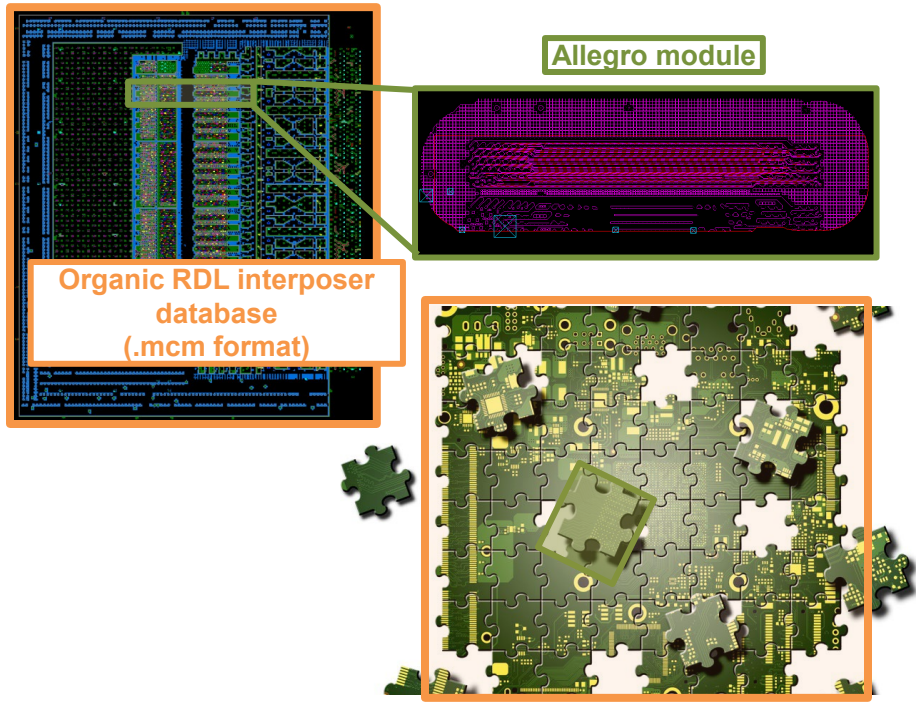
Algorithmic Selective Cutting Methodology Proposition

Design platforms (Allegro X PCB and Packaging)

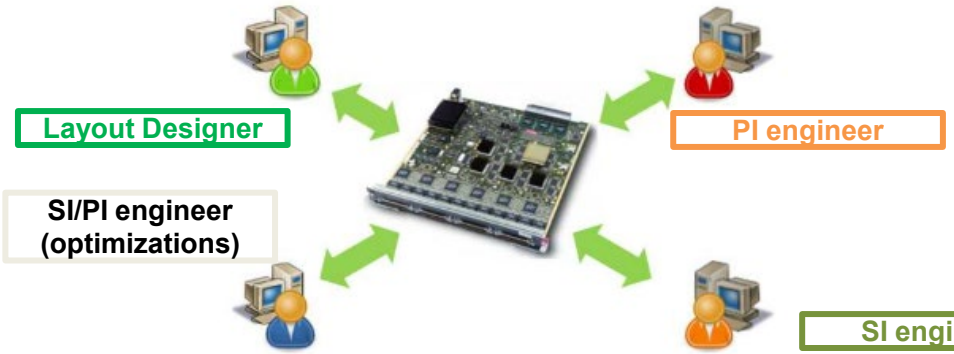
- Layout databases (.sip, .mcm) need to be translated to the Sigrity™ file (.spd) format for extraction.
- Large designs or databases with many degassing holes or challenging geometries can take hours to be translated.
- **Algorithmic Selective Cutting:** Allegro® X and Allegro X Package Designer enhancements that enable the partitioning and stitching together of a layout design.
  - Design will be cropped per user selected nets/margin, then translated.
  - Reduces the translation time and accelerates the SIPI extraction setup and overall runtime to get results.
  - Creates **module files** that can be shared across different teams (layout designers, SIPI engineers) and optimized and reapplied at the master design level.

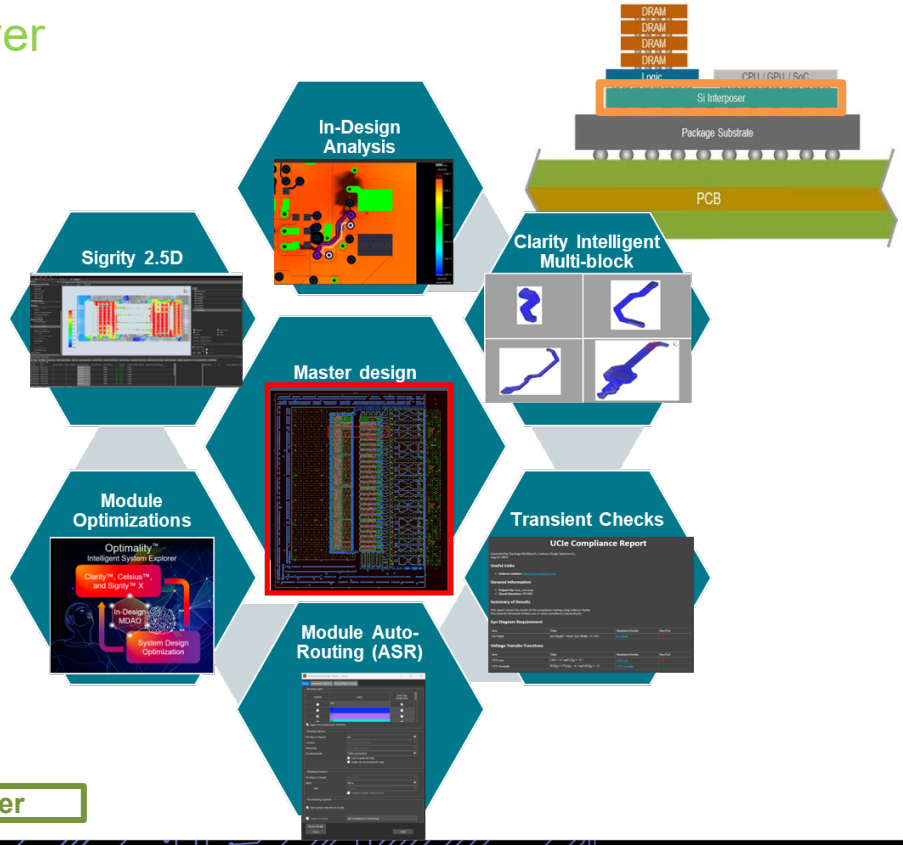


Algorithmic Selective Cutting Methodology

Analysis, Sigrity technology, Clarity 3D Solver

- Rapid and efficient translation enables automation flows with Sigrity™ and Clarity™ solvers:
  - In-design analysis (IDA)
  - Classic SI/PI extraction workflows (2.5D and 3D)
  - Transient checks
  - Module optimizations and constraints back annotation
  - Multi-fabric analysis (interposers, PKGs, and PCBs)

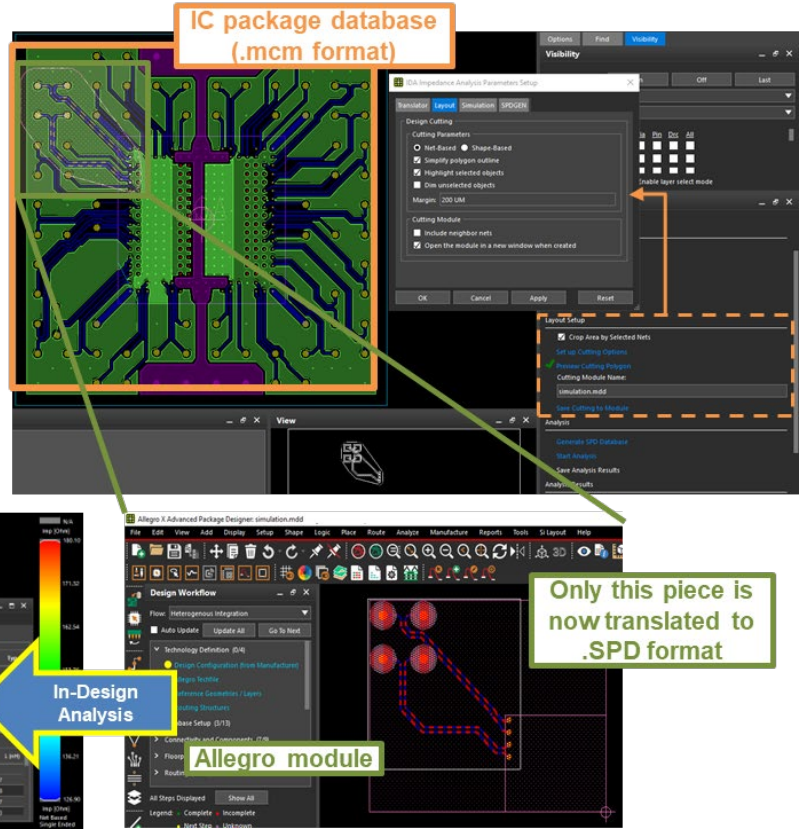




Algorithmic Selective Layout Cutting

What it is

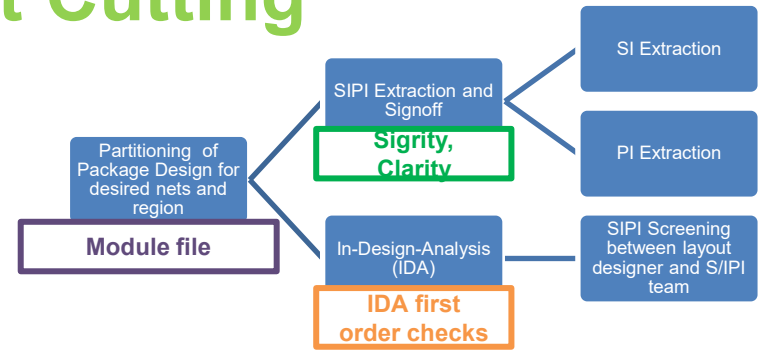
- **Algorithmic Selective Cutting:** Allegro® X and Allegro X Allegro Package Designer enhancements that enable the partitioning and stitching together of a layout design.
  - Design will be cropped per user selected nets/margin, then translated.
  - Reduces the translation time and accelerates the SI/PI extraction setup and overall runtime to get results.
  - Creates module files that can be shared across different teams (layout designers, SI/PI engineers.

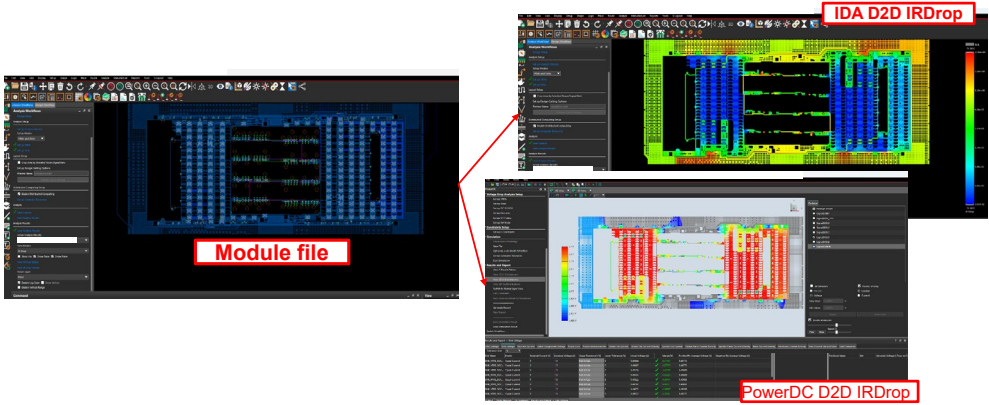


Algorithmic Selective Layout Cutting

How it benefits design and simulation

- **Traditional flow**: In-design analysis (IDA) and Sigrity™/Clarity™ extractions work by extracting the contents of Allegro® X PCB /Allegro X Advanced Package Designer databases to .spd format
  - **Translates entire design** to .spd before trimming, leading to significant time (translation, simulation setup, runtime) and memory wasted
- **New flow**: before translating, generate a pre-cut Allegro DB, including the objects needed
  - Result is **much smaller design, extremely fast .spd file generation**
- Bypass mode: Real-time design cut and margin preview prior to spd file generation
- Module mode: Real-time design cut, margin preview and module creation prior to spd file generation

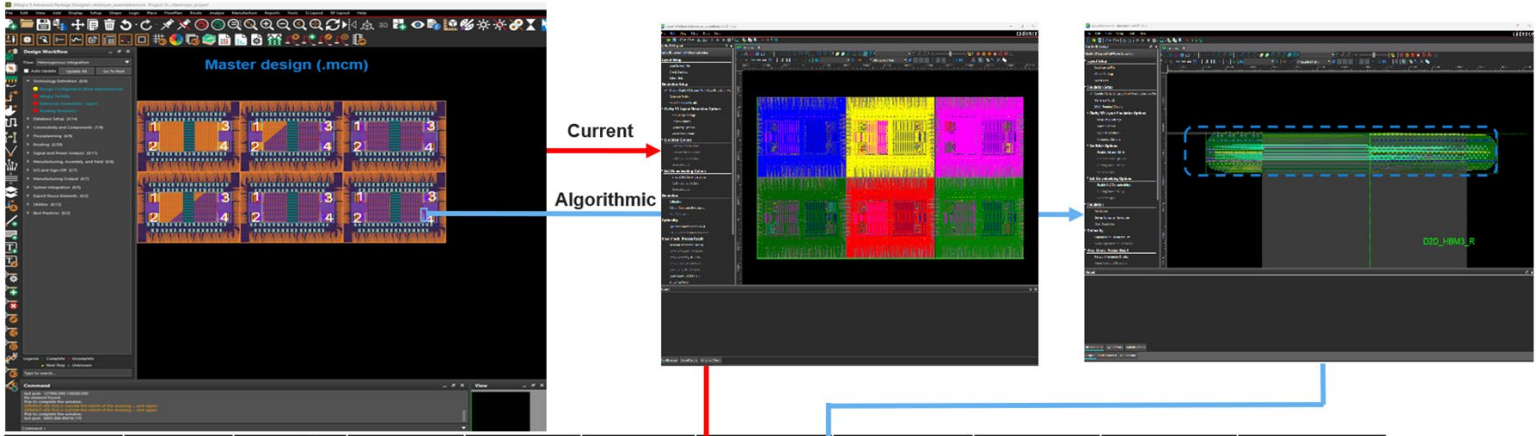




Algorithmic Selective Layout Cutting

Benchmarks

- D2D sample Impedance profile: 8 ASIC's, 24 HBME3s, 1100 IPD caps, 503000 design structures (PG, signal), 13.4M vias, 51,000 Pkg balls

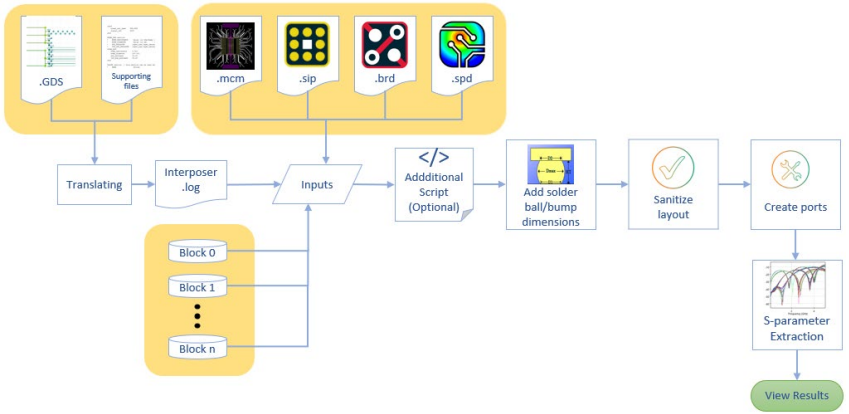


Test	mcm (on disk)	module (on disk) Algorithmic	spd (on disk)	spd (on disk)	Memory (peak)	Wall time	TAT	Memory Reduction	spd size reduction	Layout size reduction (module)
Current	8.6GB	---	21GB	---	246GB	3:58:00	---	---	---	---
Algorithmic	---	1.94MB	---	1.96MB	787MB	0:00:19	752X	320X	10714X	4433X

Intelligent Multi-Block Extraction

Motivation, What it is

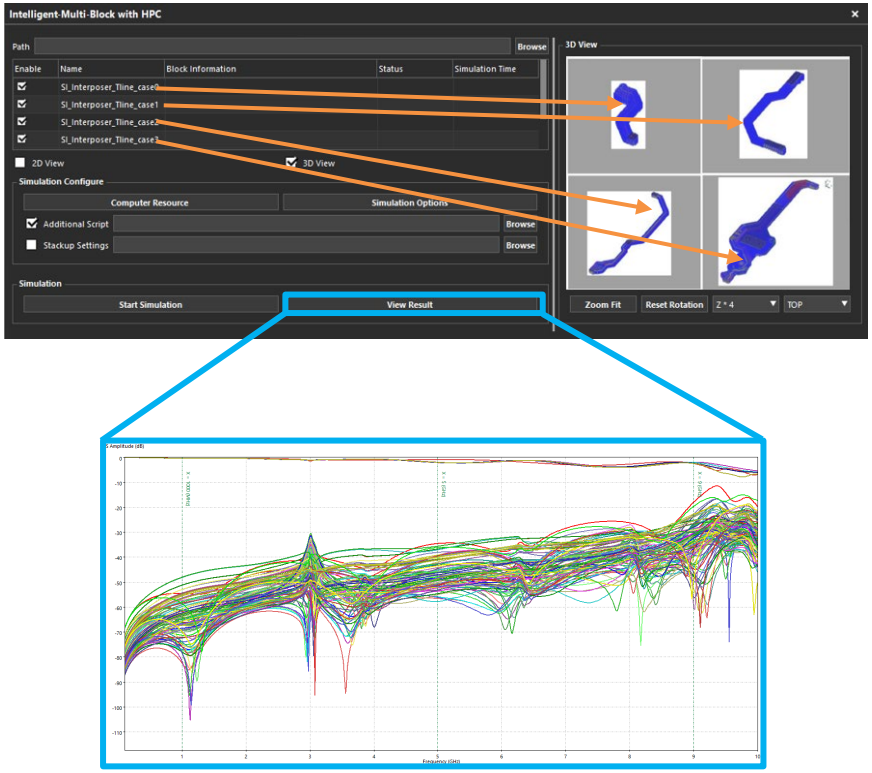
- Clear need to better integrate the layout of interposers, IC packages, and PCBs to extraction and analysis engines
  - More extractions needed earlier in the design cycle
  - **Translation** and **runtime** are critical to accelerate analysis and optimizations
- Growing design complexity stressing translations, model preparation for extraction
  - How to address this intelligently to feed our high-capacity solvers?
- Intelligent multi-block extraction
  - Once a layout file is translated, smaller blocks can be created for rapid simulation
  - Automatically **cut the simulation file into smaller blocks**, create ports and settings for each block, starts and monitors **simulations in parallel**



Intelligent Multi-Block Extraction

How it benefits analysis

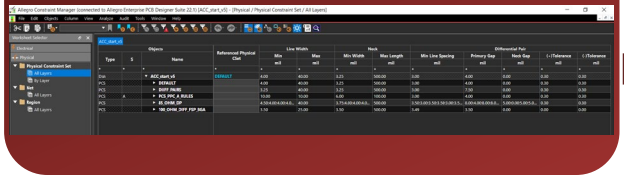
- Automatically **cut simulation file into smaller blocks**, create ports and settings for each block, starts and monitors **simulations in parallel**
  - Thus, the overall turnaround time reduces for improvements in **translation time** and **runtime**
- Having consistent, reliable extractions is key to enabling data mining and analysis comparing design iterations, previous tapeouts, measurements correlations, etc.
- Establishes traceability and creates design references



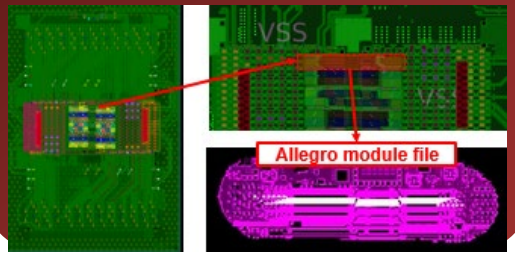
AI-Driven Design Synthesis with Constraints

Pre-layout analysis

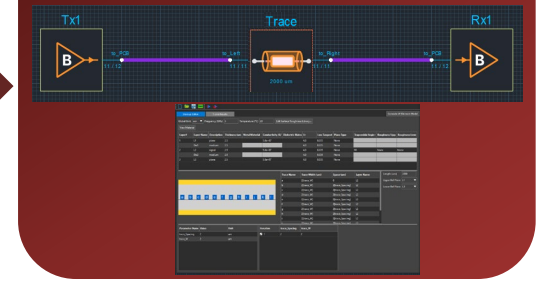
Allegro® X/APD Constraint Manager



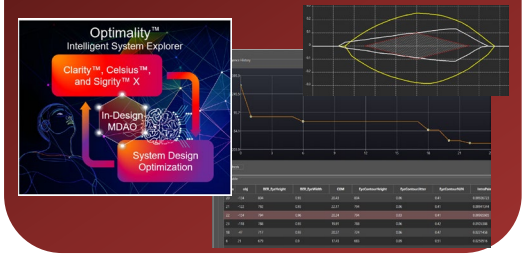
Allegro X/APD/Sigrity™ Aurora Design



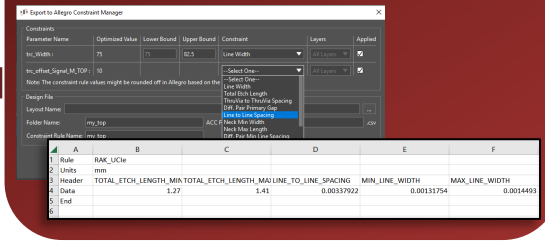
Sigrity Topology Workbench



Optimality™ Explorer

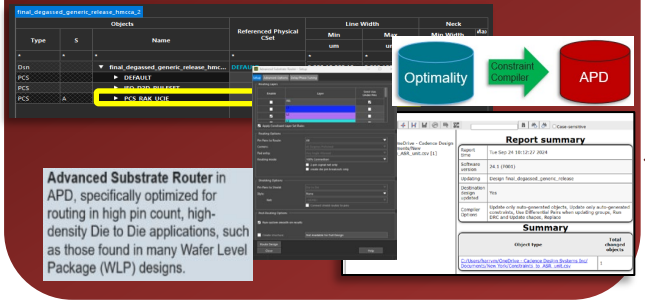


New Constraint Set Generation



	A	B	C	D	E	F
1	Rule	RAK_UCIe				
2	Units	mm				
3	Header	TOTAL_ETCH_LENGTH_MIN	TOTAL_ETCH_LENGTH_MAX	LINE_TO_LINE_SPACING	MIN_LINE_WIDTH	MAX_LINE_WIDTH
4	Data	1.27	1.41	0.00337922	0.00131754	0.0014493
5	End					

Allegro X/APD Constraint Compiler and Advanced Substrate Router

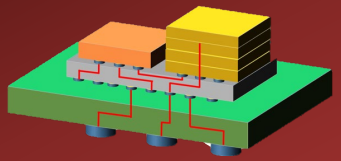


Advanced Substrate Router in APD, specifically optimized for routing in high pin count, high-density Die to Die applications, such as those found in many Wafer Level Package (WLP) designs.

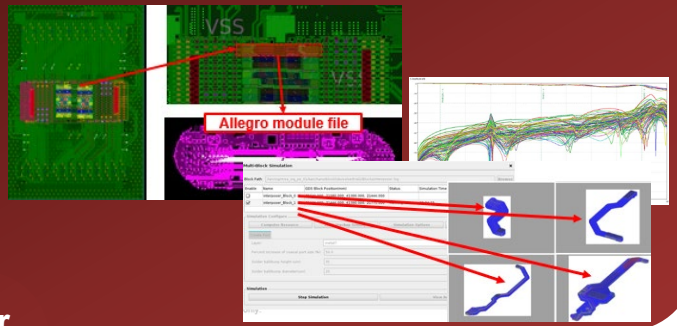
System-Level SI Post-Route Optimization Methodology

Post-route analysis

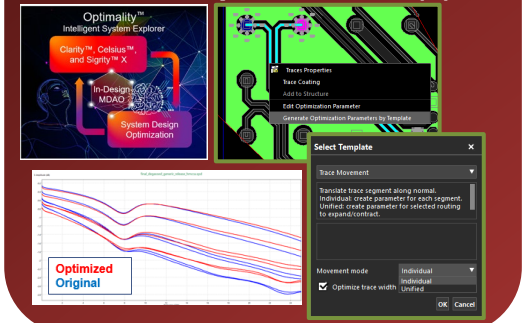
Routed interposer and PKG



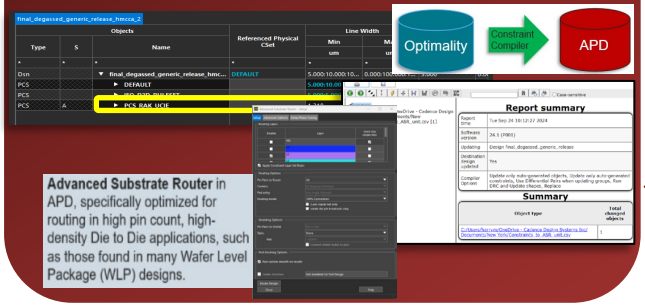
Intelligent Cuts and Parallel Extractions



Module Optimizations (1)



Allegro® X/APD Constraint Compiler and Advanced Substrate Router



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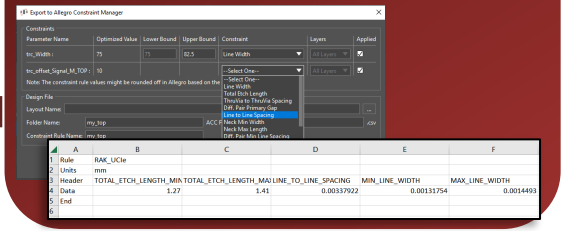
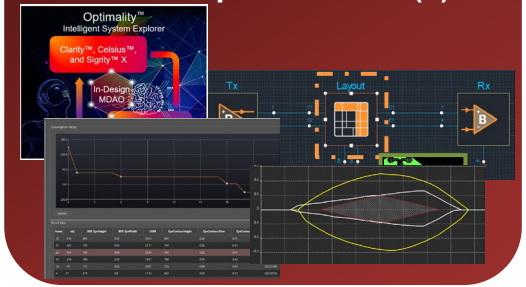
New Constraint Set Generation



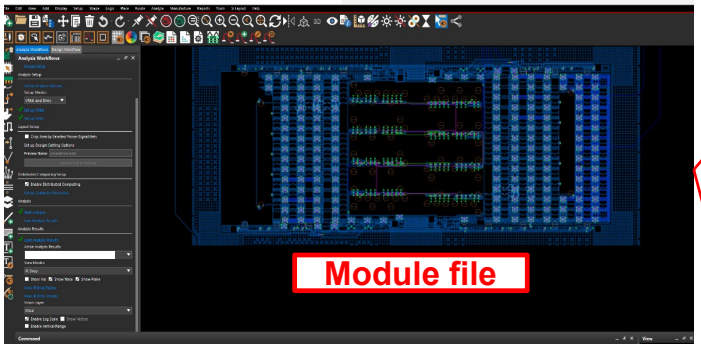
Module optimizations (2)

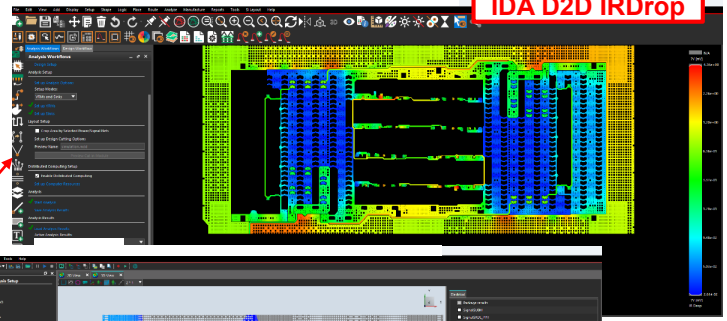


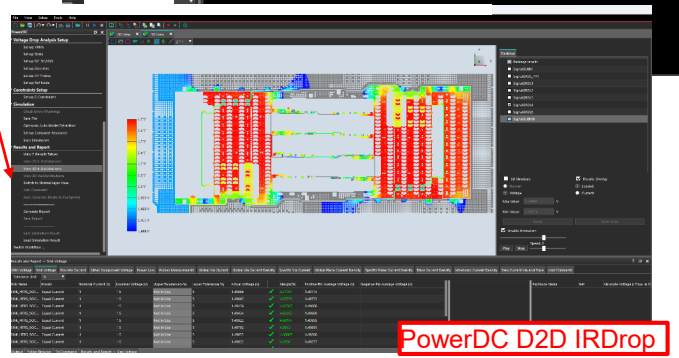
PDN Analysis

Die-to-die IR-drop example

- Layout-based cut preview quickly identifies “analysis area” prior to analysis launch
- Quick 3D viewing and PI fine tunning
- Optimized changes can be annotated back to main design

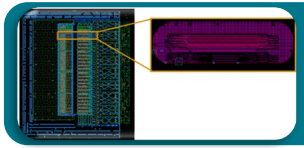






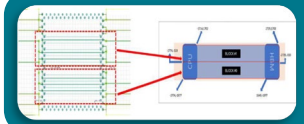
Heterogeneous System Extractions

Multi-fabric analysis of interposers, IC packages, and PCBs



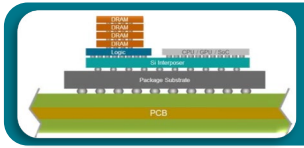
Interposer/PKG Design Cropping

- Group Relevant Nets and Areas for SI/PI Analysis
- Define cutting regions and margin
- Crop layout as desired with output .mcm, etc.



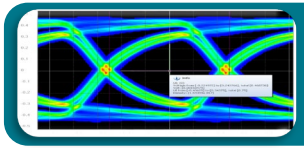
Translation of target analysis nets and area

- Translate already cropped GDS/MCM/SIP files
- Model cleanup and translation for SIPI Analysis
- **Vastly reduced translation runtime and allows for easy sharing of IP blocks for SIPI analysis**



Interposer/PKG Multi Block Analysis Automation

- Batch mode extraction of nets
- Define common ports, extraction setup
- **Traceability: Consistent results and enables easy comparison to previous Tapeouts or design iterations**



Verification of System Performance w/ Spectre

- Channel analysis with SystemSI

Optimization/Monte Carlo/Statistical Analysis: via translations, decap placement, routing, etc.

- Reduce to smaller .spd files for deeper analysis and to reduce runtime
- Provide constraints and run in Optimality
- Pass back constraints to Layout Designers for review

Conclusion

- High-performance computing chip designs challenging translators and layout tools
- Keys to success: **Parallelization**, **integration,** and **Turn-Around-Time (TAT)**

Algorithmic Selective Cutting

- Enables partitioning and stitching together of layout design
- Reduce **translation time** and accelerate **SIPI extraction setup and overall runtime** to get results
- Rapid and efficient translation enables automation flows with Sigrity™ and Clarity™ solvers
- Edits made to module can be reapplied to original layout database

Intelligent Multi-Block Extraction

- Automatically **cut simulation file into smaller blocks**, create ports and settings for each block, starts and monitors **simulations in parallel**
- Overall turnaround time is reduced
- Consistent, reliable extractions enable data mining and analysis
- Establishes traceability and creates design references

Conclusion and Next Steps

- Algorithmic Selective Cutting and Intelligent Multi-Block extraction methodologies enable flows such as:
  - AI-driven design synthesis with constraints
  - System-level SI post-route optimization
  - Multi-fabric analysis of interposers, IC packages and PCBs
- Provide your design teams with the ability to:
  - Distribute layout and analysis efficiently within scalable workflows
  - Integrate layout of interposers, IC packages and PCBs within simulation and analysis domain (**multi-fabric analysis**)
  - Run more extractions needed and earlier in design cycle
- Algorithmic selective layout cutting methodology implemented in other layout tools
  - Facilitates layout file stream out: directly exports .spd file (considering the cuts) instead of GDS, no need for supporting files (tech and map files)

Thank you!

QUESTIONS?

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Conclusion and Next Steps

- High-performance computing chip designs have been challenging translators and layout tools given the growing scale of engineering designs.
- Need to provide design teams the ability to:
  - Distribute the layout and analysis efficiently within scalable workflows.
  - Integrate the layout of interposers, IC packages and PCBs within the simulation and analysis domain (**multi-fabric analysis**)
  - Run More extractions needed and earlier in the design cycle
- **Parallelization**, **integration,** and **Turn-Around-Time (TAT)** are key to success.
- Algorithmic Selective Cutting in Allegro and APD enables the partitioning and stitching together of a layout design (module-based approach).
  - Reduces the translation time and accelerates the SIPI extraction setup and overall runtime to get results.
  - Rapid and efficient translation enables automation flows with Sigrity™ and Clarity™ solvers.
  - Edits are made to the module can be reapplied to the master layout database
- Intelligent Multi-Block extraction
  - Automatically cut the simulation file into smaller blocks, create ports and settings for each block, starts and monitors simulations in parallel
  - Overall turnaround time is reduced for the improvements in the translation time and runtime
  - Consistent, reliable extractions enable data mining and analysis comparing design iterations, measurements correlations. Establishes traceability and creates design references.

Conclusion and Next Steps

- Algorithmic Selective Cutting and Intelligent Multi-Block extraction methodologies enable flows such as:
  - AI-Driven Design Synthesis with Constraints
  - System-Level SI Post-Route Optimization
  - Multi-fabric analysis of interposers, IC packages and PCBs
- Algorithmic selective layout cutting methodology to be implemented in other layout tools (**Innovus™ Implementation System**)
  - Facilitates the layout file stream out: directly exports .spd file (considering the cuts) instead of GDS, no need for supporting files (tech and map files).