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Simulation Next-Gen AI Interconnects: Optimizing to 448 Gb/s and Beyond

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SPEAKERS

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Raul Stavoli manages SI/PI analysis and design of high-speed interconnects spanning chip, package, board, and cable assemblies at Rosenberger North America. He holds a Bachelor of Science in Electrical Engineering from San Francisco State University (2014). Prior to RosenbergerNA, Raul led the SI/PI Applications Engineering team at Cadence Design Systems supporting hyperscaler and data center customers. These applications require high-speed serial links, power delivery networks (PDN), and system-level co-simulation workflows. In RosenbergerNA, he is responsible for the design and validation of high-speed digital and RF interconnect solutions for automated test equipment (ATE), data center, and aerospace/defense applications.

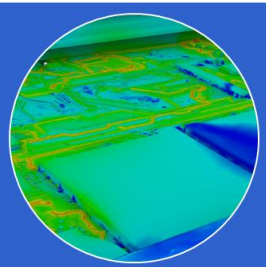
Outline

- Manufacturing & Simulation Production Workflows
  - 3D Field Solver
  - Machine Learning/ AI Optimization Engine
- Test Fixture Design for 448 GB/s
  - RF Interconnect Modeling & Validation
  - Precision Connectors
  - Test Fixture Validation & Review

High-Level Signal Integrity Workflow

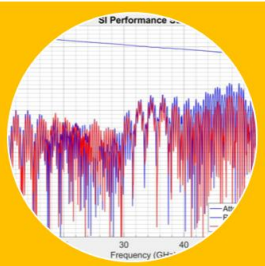
Interconnect Mechanical Design

- Product target performance/specs defined
- 3D model shared with SI team (.step, .sat)
- Material Properties Definition (Dk, Df, thermal)
- Database Translation (to ANSYS, Sigrity, CST)
- Identify critical manufacturing features and areas where optimization is possible



Electro-Magnetic 3D Modeling

- Parametrize model as needed.
- Define excitations/port and components
- Define extraction configuration (freq sweep, boundary conditions, etc.)
- Run 3D Field solver
- Scan/extract PCB only with 2.5D Solver
- Simulation first different elements of the channel then the full channel for validation
- Interconnect Only, PCB Launch/Breakout, Cable, etc.



Post-Processing Results

- Review S-Parameter Models, Time Domain Reflectometry, EM fields, SPICE model
- Characterize if interconnect meets target specifications.
- Identify areas of optimization
- Correlate results to measured data
- Document results for internal/external customers
- Create Production Testing limits (fixture dependent)

Matlab and Python Automation

Outline

- **Manufacturing & Simulation Production Workflows**
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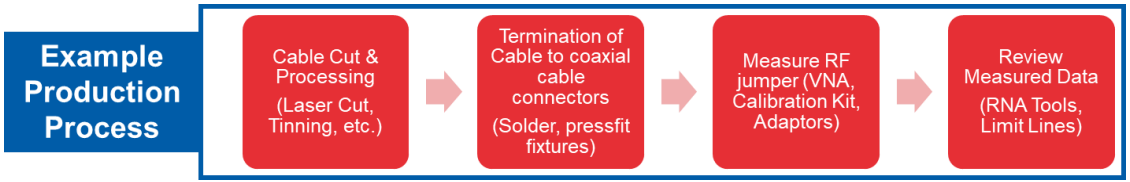
Manufacturing vs. Simulation Production Workflows

- Production Facilities (Factory)
  - Manufacturing processes, tooling, fixtures, raw materials, components, etc.
  - Operator independent processes improve yield and deliver consistency/quality.
- Manufacturing Process & Workflows
  - Key Pillars:
  - Manufacturing/Mechanical Engineering, Product Design, standardization and controlled implementation of a process
  - Successful Deployment == cost control, predictability & stability
- Same Concepts apply to Signal Integrity Production Workflow

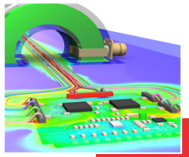


Manufacturing vs. Simulation Production Workflows

- Signal Integrity Production flow also requires tooling, fixtures to achieve consistency, scale, etc.
- Signal Integrity Tooling/ Fixture Design
  - Parametric Model of the interconnect and any mating assemblies (cable, PCB, other interconnect)
  - A parametric model is an abstract model than enables the rapid modification of geometry.
  - 3D Field Solver (accurate and reasonable runtime)
  - Validation of extracted performance vs. the target specification.
  - Consistent Material library, extraction settings (excitations, boundary conditions, etc.) and database of simulated data (SParameters)
- Artificial Intelligence/ Machine Learning (AI/ML)
  - Enables operator independent basic signal integrity production workflows
  - Limited/Constrained Solutions Space

Manufacturing / Production

- **Manufacturing Process**
- **Input:**
  - Components/Assemblies
- **Validation:**
  - VNA, Optical Inspection
- **Output:**
  - Finished Interconnect and Cable Assemblies, Documentation
- **Production Fixtures/Equipment**
  - Laser Cut
  - Tinning
  - Solder Station
  - Hot Bar
  - Press fit Fixtures
  - Assembly Fixtures

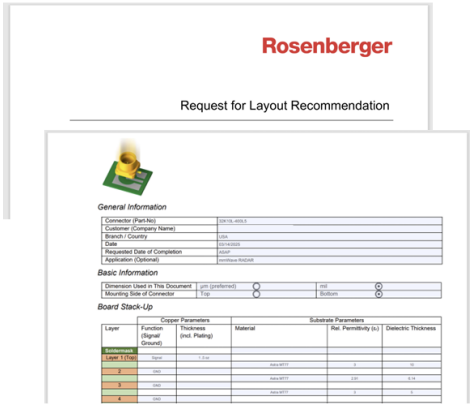


Signal Integrity Workflow

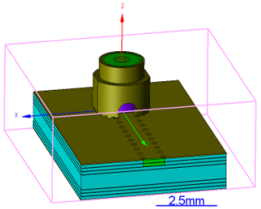
- **Signal Integrity Workflow**
- **Input:**
  - 3D Component Models, Assembly Model (cable, PCB)
- **Validation:**
  - 3D Field Solver
- **Output:**
  - Optimized Interconnect and Cable Assemblies, Documentation
- **Production Fixtures/Equipment**
  - Parametric Models
  - Cascading Engine
  - High-Performance Computing Resources

Creating a SI “Tooling/Fixture” Design

1) Customer Layout Request

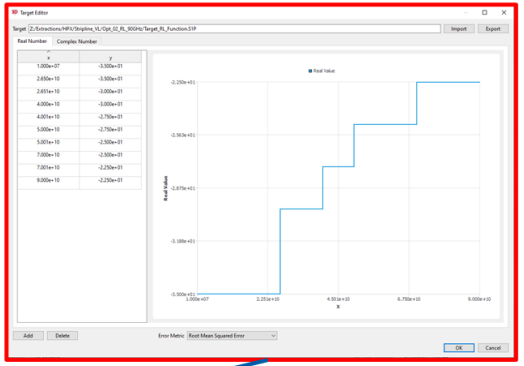


2) 3D Interconnect Model & Configuration
(Vertical/edge launch, etc.)

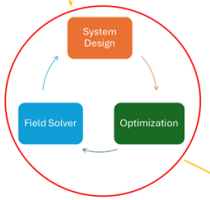


Index	Optimize	Name	Type	Expression	Ref Value	Unit	BoundType	LowBound	HighBound
1	☑	L1_Antipad_Diameter	continuous	0.95 mm	0.95	mm	absolute	0.76	0.95
2	☑	L2_Antipad_Diameter	continuous	0.82 mm	0.82	mm	absolute	0.75	0.82
3	☑	Signal_Spacing_Trace2CPW_Breakout	continuous	0.21 mm	0.21	mm	absolute	0.12	0.23
4	☑	Signal_Trace_Breakout_Length	continuous	0.4 mm	0.4	mm	absolute	0.2	0.6
5	☑	Signal_Trace_Breakout_Width	continuous	0.14 mm	0.14	mm	absolute	0.1016	0.2
6	☑	Signal_Trace_Taper_Base_Length	continuous	0.3 mm	0.3	mm	absolute	0.2	0.8
7	☑	L3_Antipad_Diameter	continuous	0.6 mm	0.6	mm	absolute	0.5	0.82

3) Optimization Target
Customer request + RNA engineering



Design Variables
Objectives
Constraints



Optimized Design

Signal Integrity Tooling / Fixture

- Parametric Model VL Stripline/CPW, EL, etc.
- 3D Field Solver
- Post-Processing Results to compare vs. target data (AI/ML, Matlab Tools)

4) Output: Optimized Interconnect Footprint and Report
(for customer and internal/database)

Evaluating EDA Tools & Workflows

- RNA Model Databases (to be consumed by field solver)
  - Layout Databases: Allegro (.brd or ODB++)
  - Mechanical CAD: Creo, some solid works
- Model setup time = sum of (the translation time, model editing, material assignment, excitations, boundary conditions, etc.)
  - The goal is to: 1) minimize setup mistakes, 2) minimize Model setup time and 3) build the foundation for automation
- Reporting time = documenting the 3D model, simulation setup, field plots, 2D graphs and analysis/feedback.
  - The goal is to: 1) minimize the time to document the model in the EDA tool. Capture excitations, images and results with some semi-automation.
- Database management: possible to leverage field solvers in layout tools? Or pass parametric properties to layouts? Show results in layout tool? Essentially any connections between EDA tool and our layout/modeling tools?

Features/Capabilities	Vendor A
Field Solver	?
Accuracy	?
Scalability/Runtime	?
Database management	?
Post-Processing	?
Integration: Layout	?
Integration: 3D Model	?

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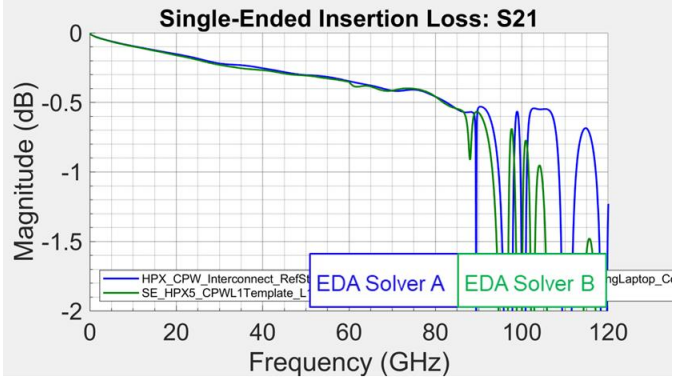
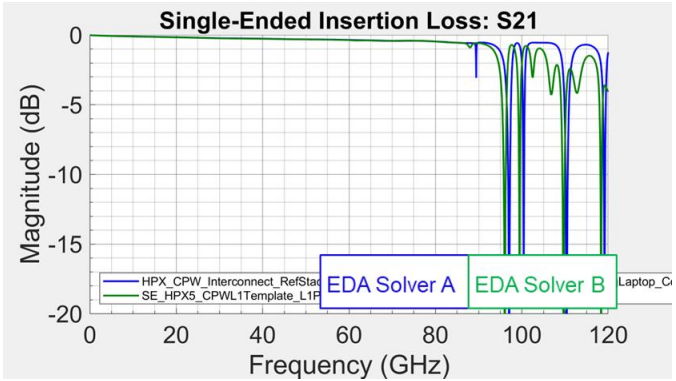
3D and 2.5D Field Solvers

Solver	Applications	Use Case and benefits
3D Finite-Element-method (FEM)	Interconnects, PCBs, Packages, IC, Antennas, etc.	• Most versatile solver • “golden standard” accuracy • Long runtimes, requires many compute resources • Each simulation can capture many ports (ideal for larger channel configurations) • Tetrahedral mesh
3D Finite Difference Time Domain (FDTD)	Interconnects, PCBs, Antennas, etc.	• Focused on “larger structures” (antennas, etc.) • Fast runtimes for single port simulations • Need to extract each port individually • Brick based mesh
2.5 D Hybrid Solver	Laminate structures like PCBs, PKGs, Ics, etc.	• Fastest runtimes • Limited only to planar geometries • Suited for fast tuning of PCBs and footprints • Different Geometries handled differently (Pad = equal potential, shape = FEM mesh, traces = Method of Moments (MoM)
DC Solver		• Run IR Drop and resistance measurements

Benchmarking 3D FEM Solver

- Goal: Minimize the runtime while ensuring 3D solver accuracy.
- Application: 110 GHz Interconnect Design
- Parametric models were run with the same settings, material properties, and general simulation settings.
- Extracted results show very similar results.
- Primary difference is EDA Solver A's runtime per frequency point is nearly twice as fast as Solver B.

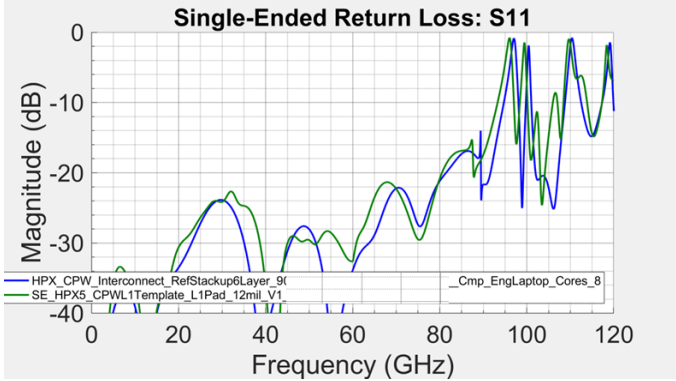


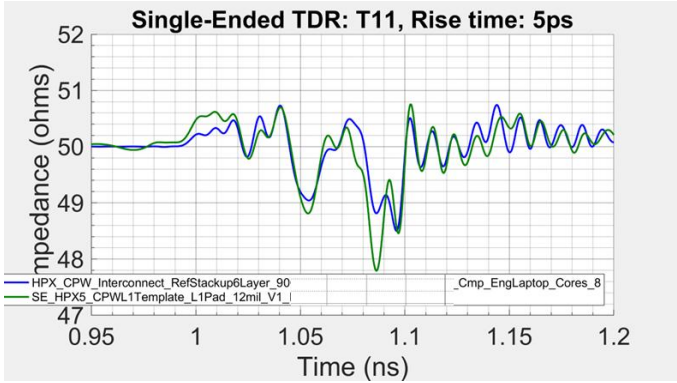


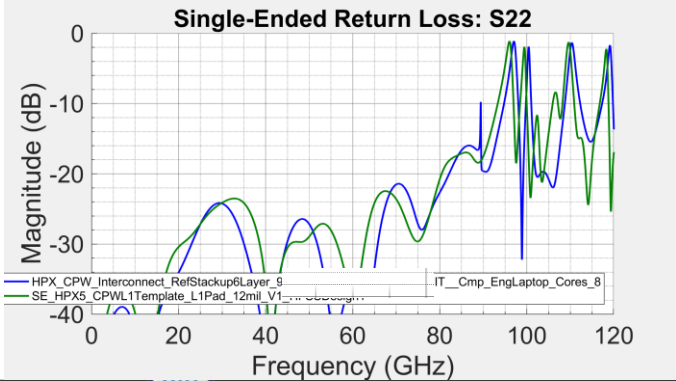
Requests Computer Resources	EDA Solver A	EDA Solver B
CPUs	8	8
RAM (GB)	64	64
Wall Time (s)	58	38
Execution Time (s)	58	56
Peak Memory (MB)	645	779
Initial Mesh	41	41
Adaptive Mesh	1192	272
# of Iterations	11	6
# of wave port iterations	6	0
Wave Port Simulation	51	0
Final Simulation (Freq Sweep)	42.3166667	47.46667
Total Simulation time	3825	3187
# of Frequencies	109	60
Time/Freq Point	0.3882263	0.791111
# of Elements	270664	292337
# of Unknowns	1349888	1349888
# of Ports	2	2
# of Near Field Freq Pts	2	1

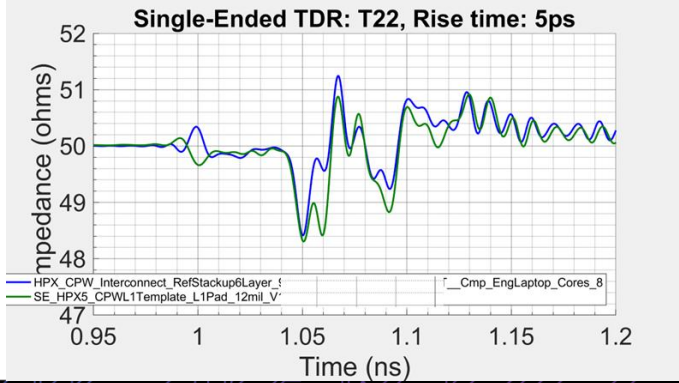
Benchmarking 3D FEM Solver

EDA Solver A | EDA Solver B

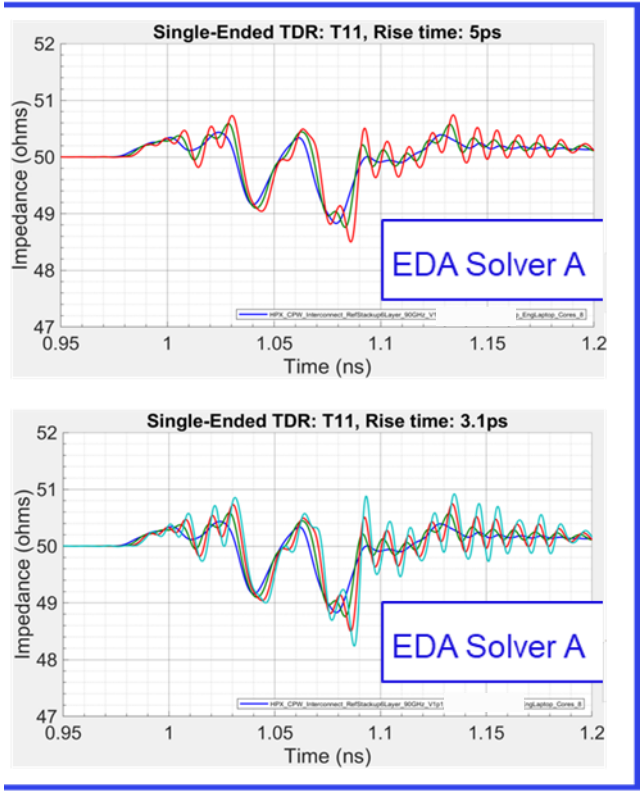


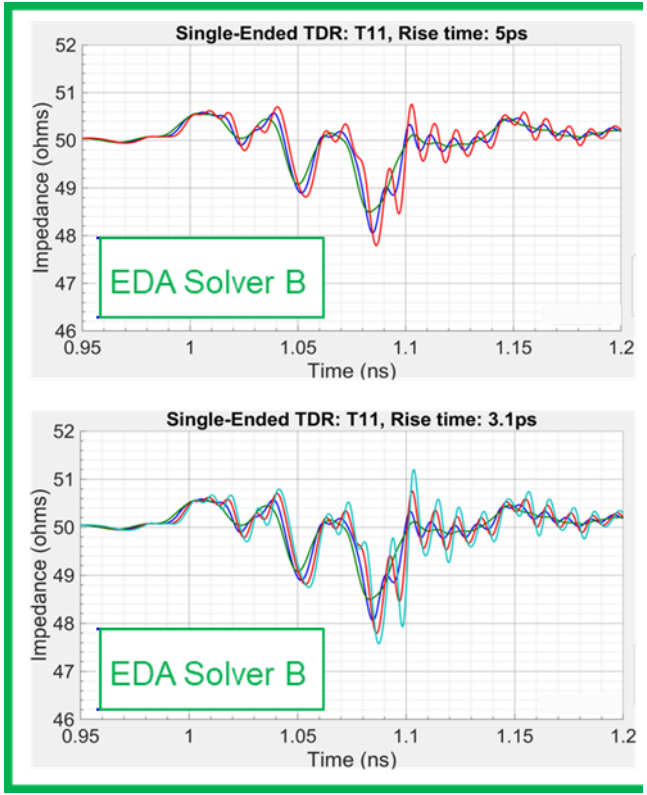






Benchmarking 3D FEM Solver





TDR Rise Time Comparison

10 ps (35 Ghz)

7 ps (50 Ghz)

5 ps (70 Ghz)

3.1 ps (110 Ghz)

Final Simulation (Freq Sweep)	42.3166667	47.46667
Total Simulation time	3825	3187
# of Frequencies	109	60
Time/Freq Point	0.3882263	0.791111
# of Elements	270664	292337
# of Unknowns	1349888	1349888
# of Ports	2	2
# of Near Field Freq Pts	2	1

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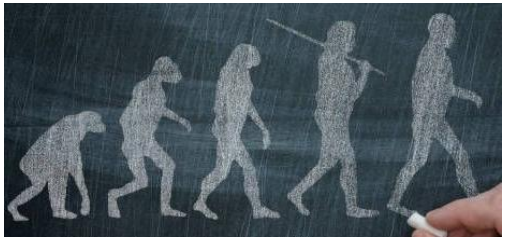
Machine Learning & “AI” Engines

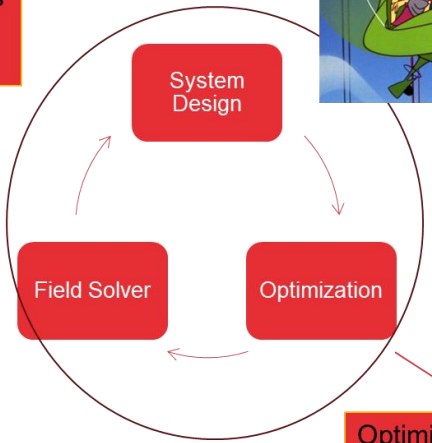
Traditional Design Optimization “Past to Current”

- Identify Design Space
- Number of possibilities
  - •6 variables * 10values
  - •1,000,000 possibilities
- Identify variables that are most sensitive
- Setup Geometry to sweep the solution space
- Run simulations for several cases
- Use engineering knowledge to identify best geometric variations



Optimality – Reinforcement Learning Enabled Optimization “Present and Future”

Design Variables
Objectives
Constraints



Optimized Design

Machine Learning & “AI” Engines

- AI / ML Engine: Bayesian Optimization
  - Step # 1: Create a Parametric Model or Parameterize Upon Import, which enables the use of:
    - *1) Machine learning and AI algorithms (geometry can be changed on the fly)*
    - *2) Optimization, Sensitivity Analysis, Robustness Correlation flow (Extract Dk and Df)*
  - Challenges:
    - *Need to properly define the variable constraints to ensure manufacturable outcomes.*
    - *Convergence of the ML/AI engine due to a large sparse solution space.*
    - *Time to create parametric model*
- Once ML/AI engine, parametric model and optimization parameters are defined this can be considered simulation “tooling”
  - new Stackup and requirements are fed as inputs to the parametric model, kicking off the optimization workflow
  - When a new interconnect is placed on the parameteric model and optimization parameters are re-defined a new set of “simulation tooling” has been created.
- Each simulation to 110 Ghz takes ~ 40minutes to 1 hour. Efficient use of resources is essential to “mine” and identify the right geometric changes to optimize performance.

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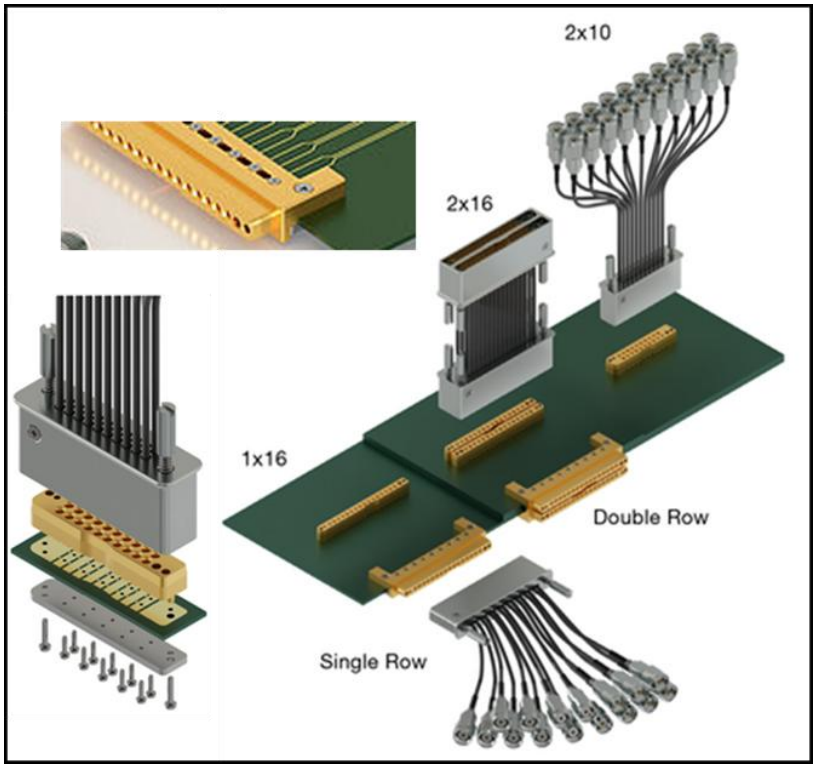
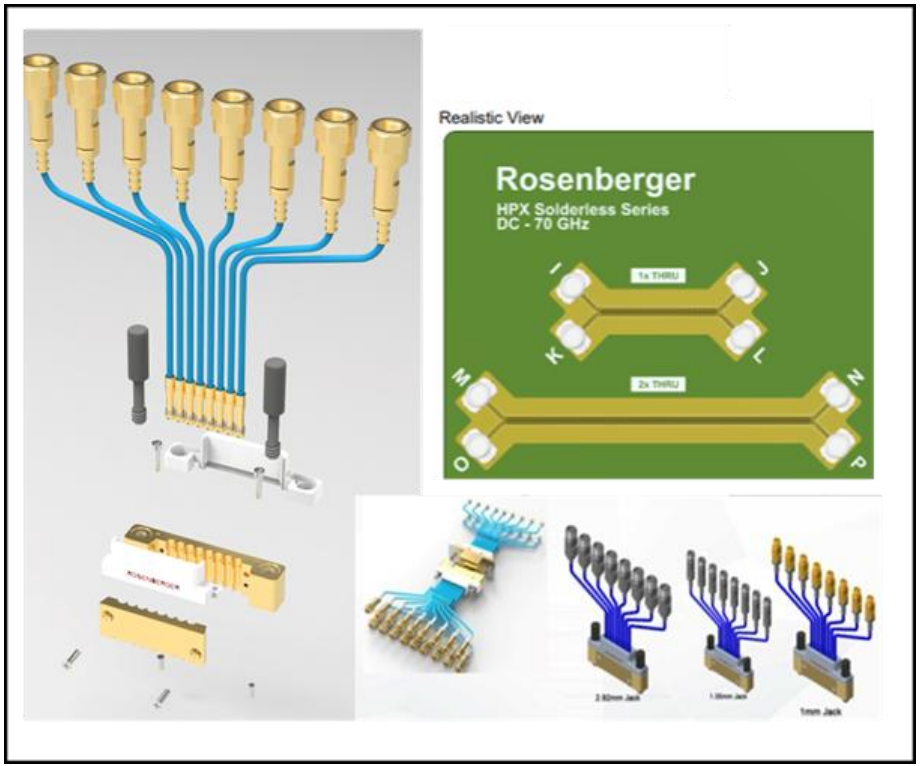
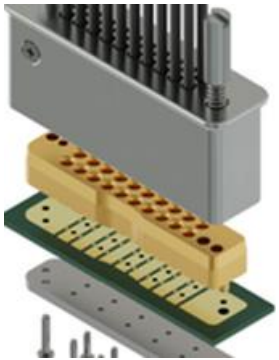
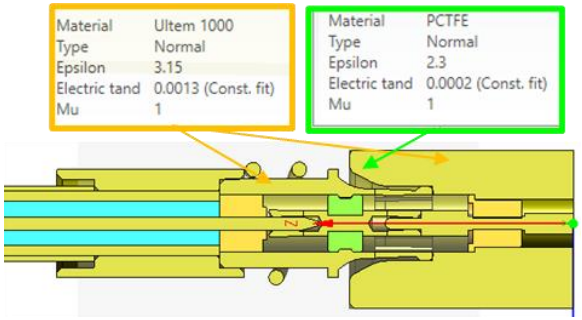
Application: 448 GB/s Interconnect Design

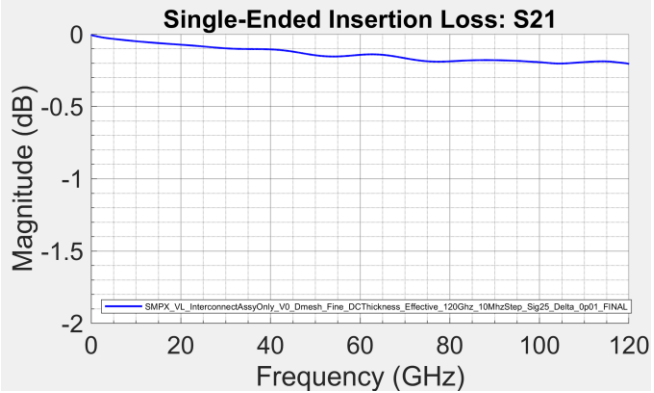


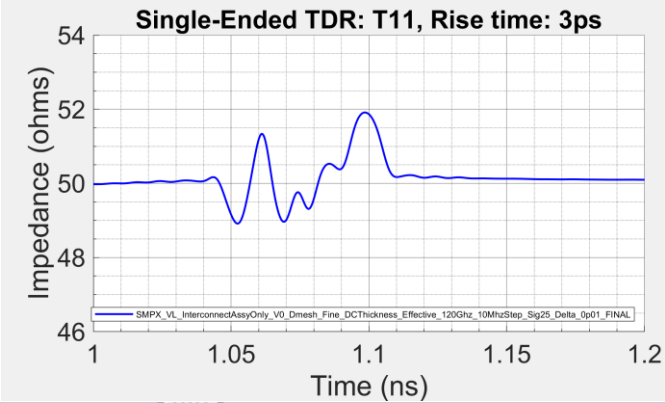


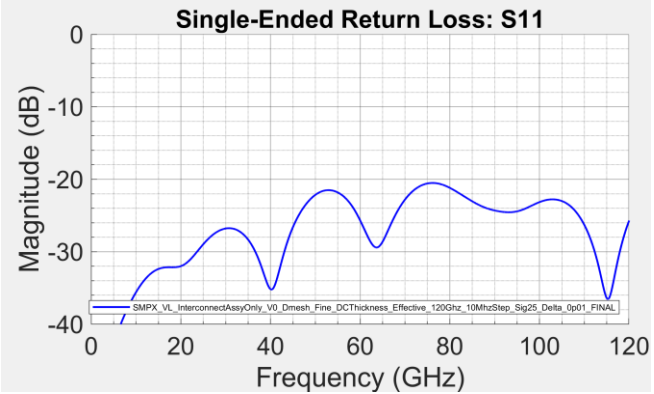
RF Vertical Launch Interconnect: Bandwidth DC- 110GHz



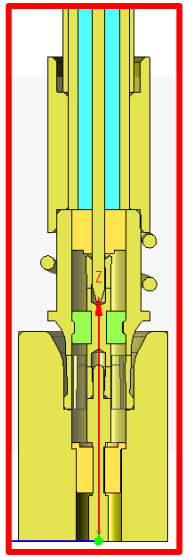


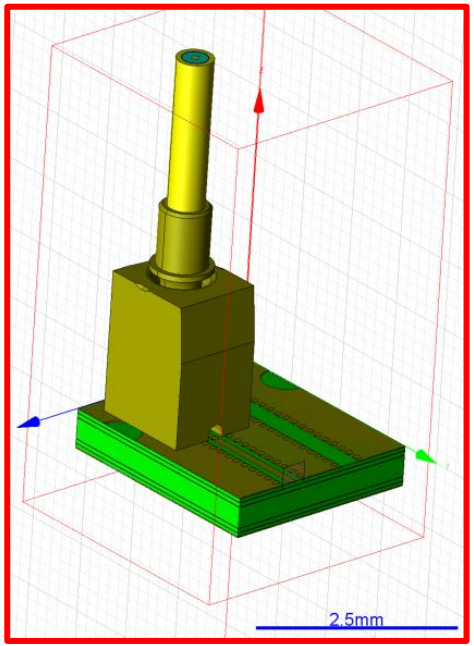


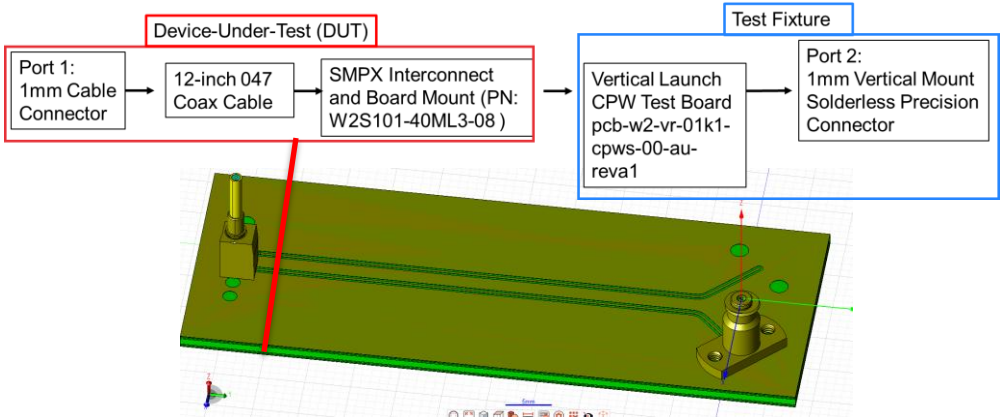


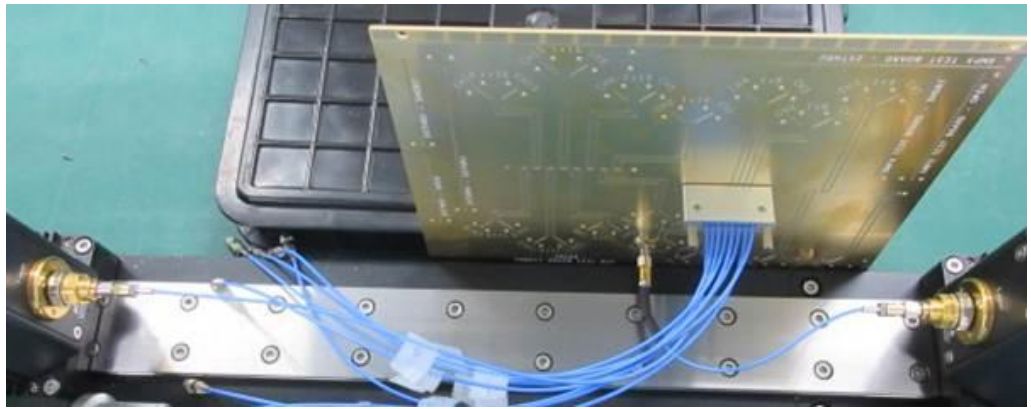


RF Vertical Launch Interconnect: Bandwidth DC- 110GHz

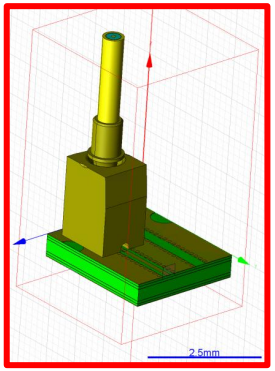


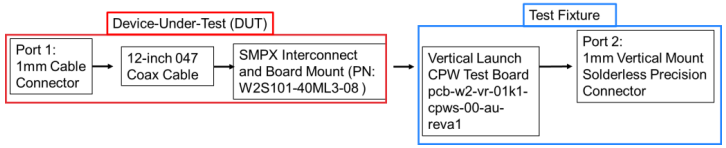


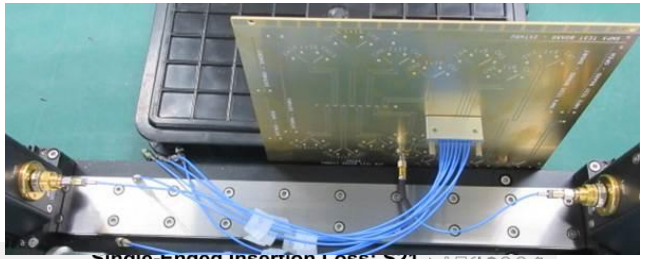


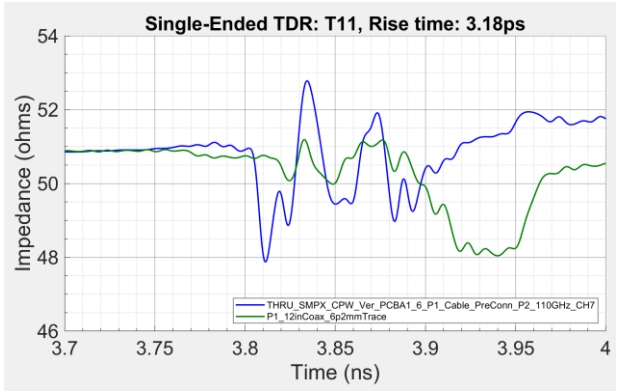


Interconnect Correlation (Measurement vs. Simulation)

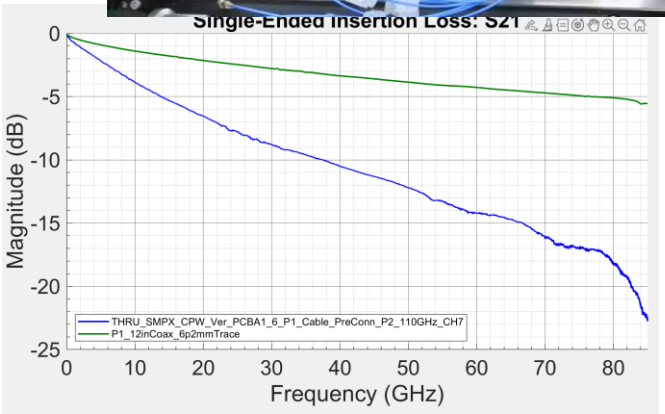


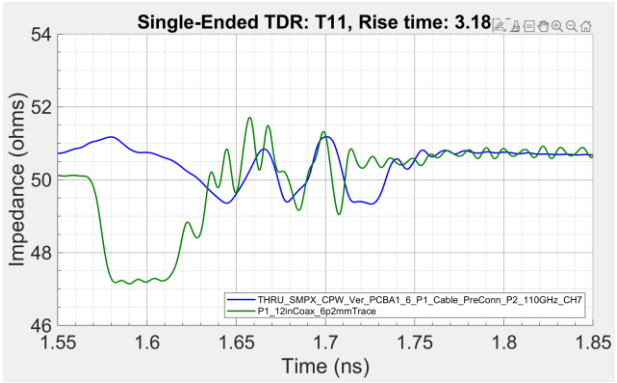




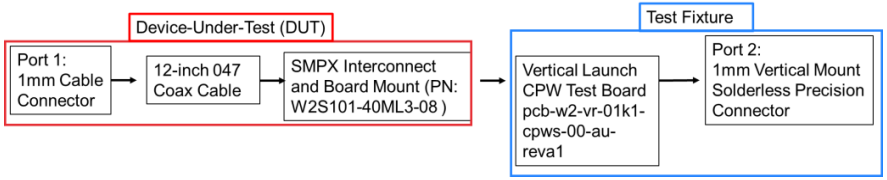


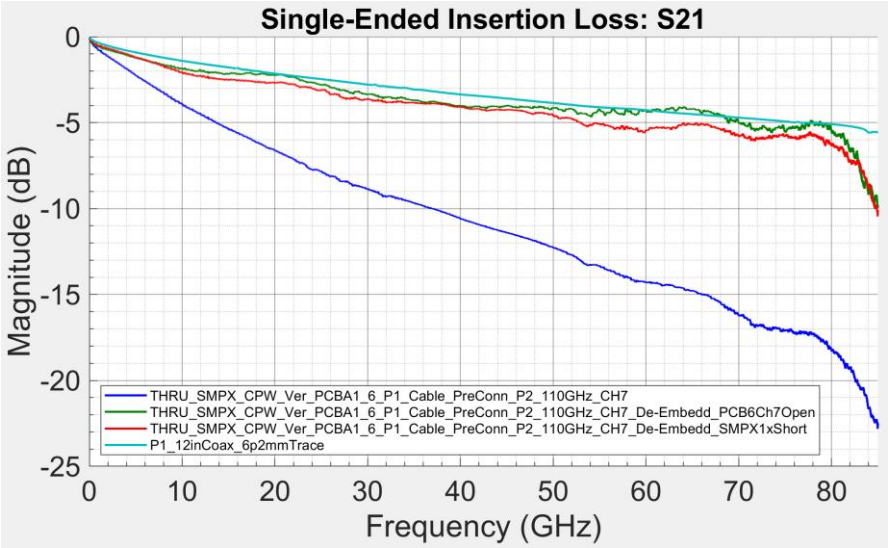
T11

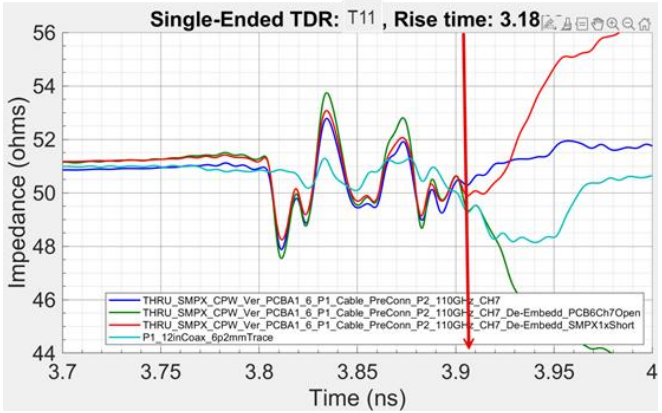


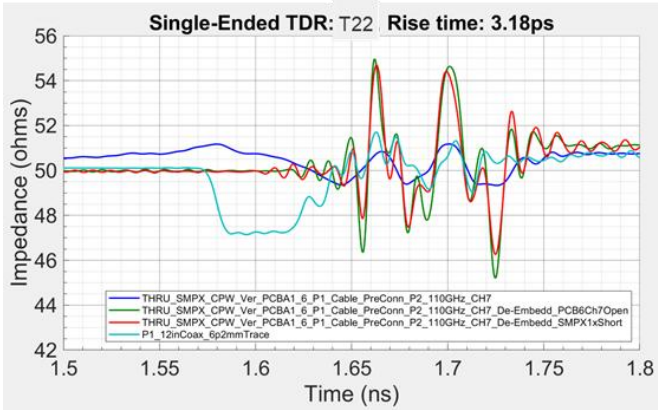


Interconnect Correlation (Measurement vs. DeEmbeded 1x Open, DeEmbedded 1x Short, Simulation)





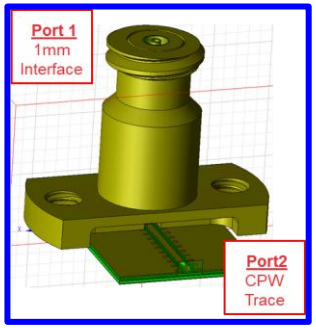




Outline

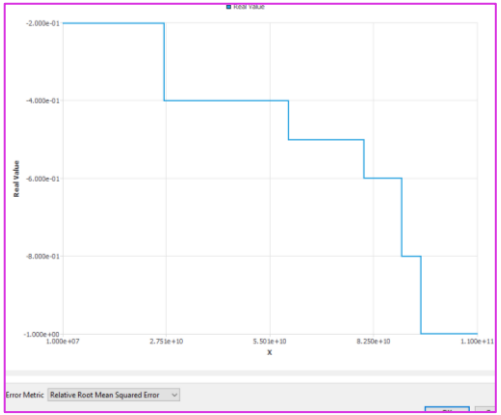
- Manufacturing & Simulation Production Workflows
  - 3D Field Solver
  - Machine Learning/ AI Optimization Engine
- Test Fixture Design for 448 GB/s
  - RF Interconnect Modeling & Validation
  - **Precision Connectors**
  - Test Fixture Validation & Review

Precision Connectors for 110 Ghz, VL



Signal Integrity Tooling / Fixture

- Parametric Model VL Stripline/CPW, EL, etc.
- 3D Field Solver
- Post-Processing Results to compare vs. target data (AI/ML, Matlab Tools)



Error Metric: Relative Root Mean Squared Error

Parameter table

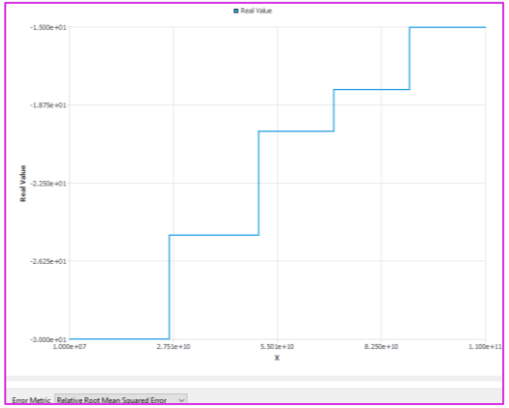
Filter

Check Parameters

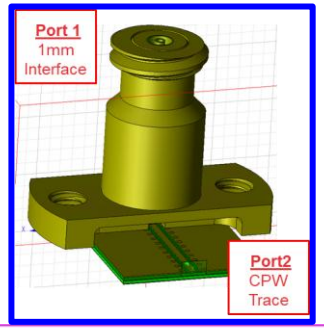
Index	Optimize	Name	Type	Expression	Ref Value	Unit	BoundType	LowBound	HighBound
1	☑	L1_Trace_Breakout_Width	continuous	0.207437 mm	0.207437	mm	absolute	0.0762	0.36
2	☑	L1_Trace_Taper_Breakout...	continuous	0.236498 mm	0.236498	mm	absolute	0.127	0.254
3	☑	L1_Trace_Breakout_Length	continuous	0.141689 mm	0.141689	mm	absolute	0.0508	0.7
4	☑	L2_Antipad_Diameter	continuous	0.61 mm	0.61	mm	absolute	0.02	0.8
5	☑	L1_Antipad_Diameter	continuous	0.655 mm	0.655	mm	absolute	0.55	0.95
6	☑	L1_Spacing_Trace2CPW_...	continuous	0.165134 mm	0.165134	mm	absolute	0.0254	0.22
7	☐	L1_Pad_Signal_Diameter	continuous	0.3048 mm	0.3048	mm	absolute	0.254	0.3048

Function table

Name	Quantity	Expression	Condition	Type	Target
IL_Measure	dB(S[1,2])		>	Measurement	Target - RRMSE
IL_Optimization		IL_Measure + RL_Measure		Objective Function(goal)	
RL_Measure	dB(S[1,1])		<	Measurement	Target - RRMSE



Precision Connectors for 110 Ghz , VL

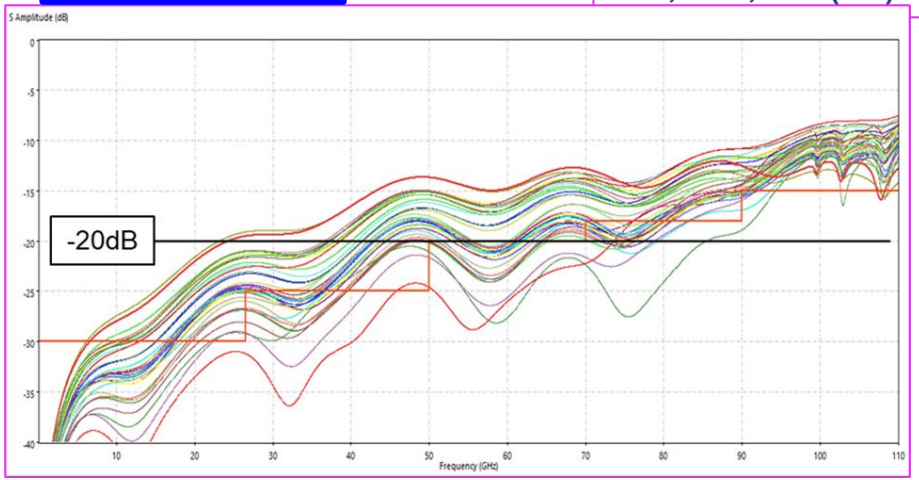


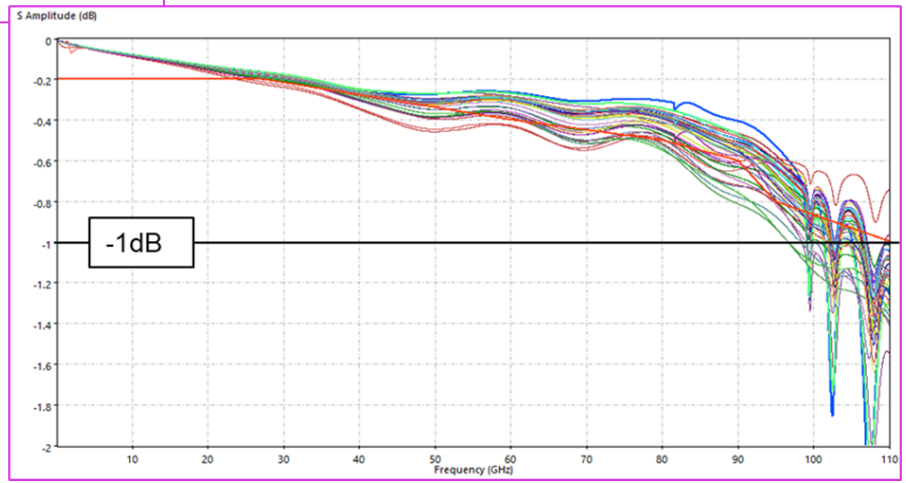
Signal Integrity Tooling / Fixture

- Parametric Model VL Stripline/CPW, EL, etc.
- 3D Field Solver
- Post-Processing Results to compare vs. target data (AI/ML, Matlab Tools)

Best Optimizations

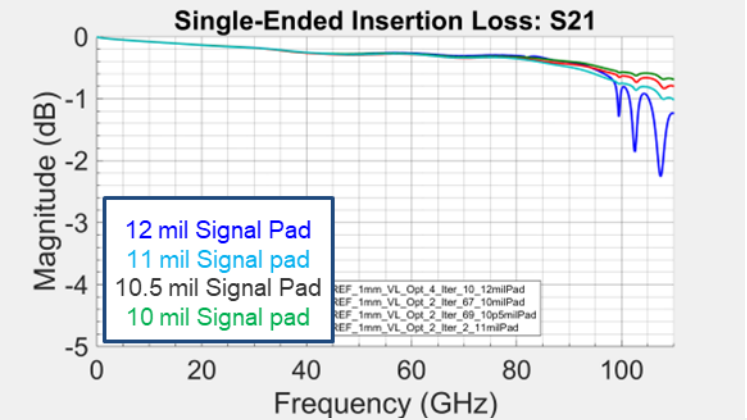
10, 28, 38(IL)

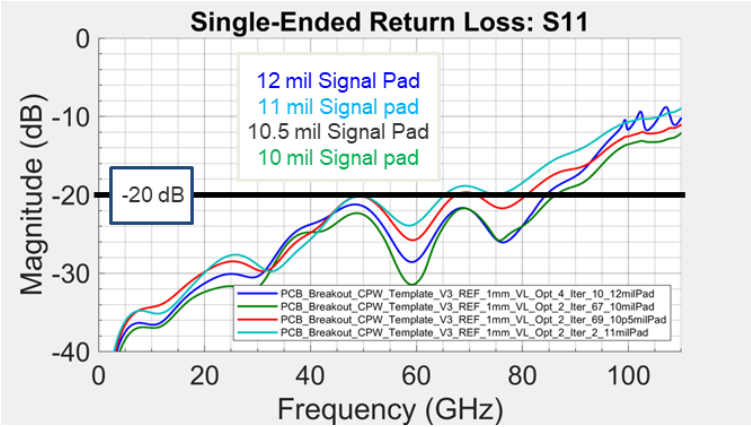


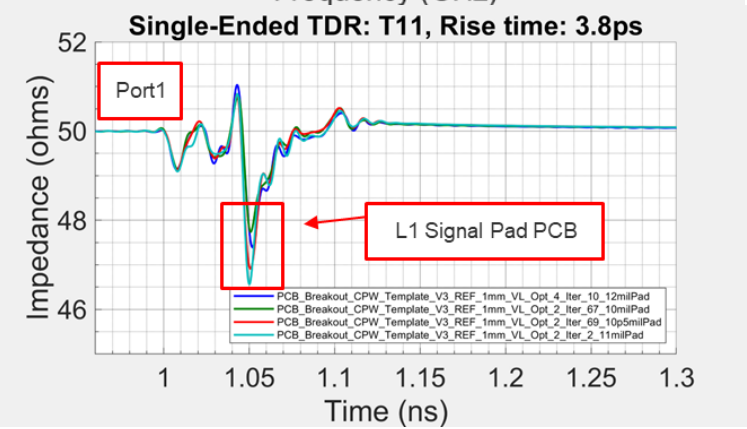


Precision Connectors for 110 Ghz , VL

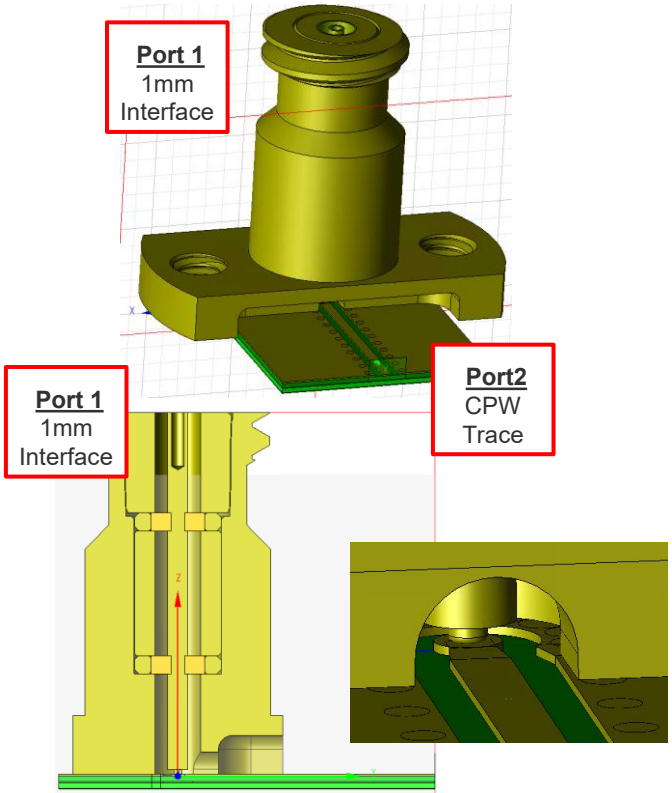
- Cadence Optimality AI/ML engine ran a parametric model with a target insertion/return loss spec line. The best manufacturable results for each pad diameter. (below)
- Going to a smaller signal pad improves the performance but reduces testing consistency (registration).
- Reflections still increase above ~90 Ghz despite the smaller signal pad and other optimizations.

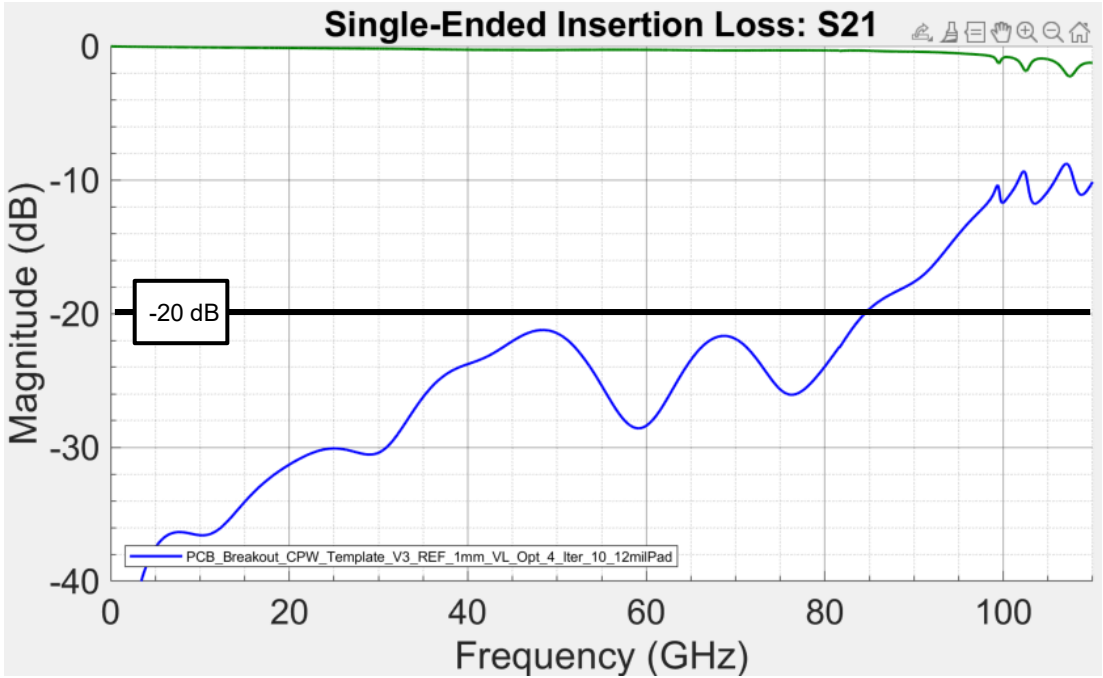






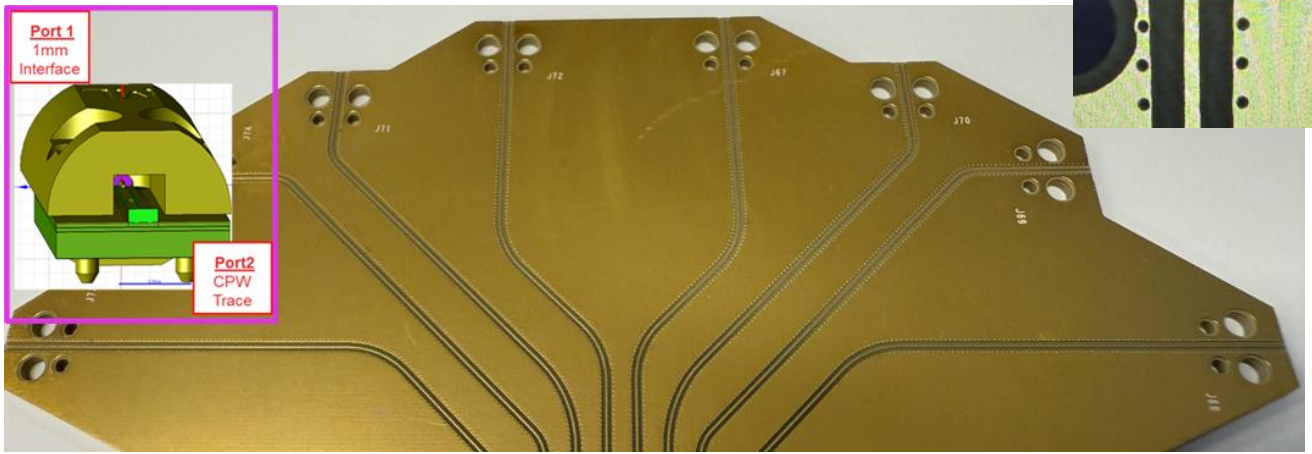
Precision Connectors for 110 Ghz , VL





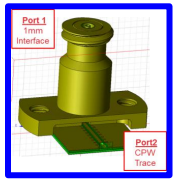
Precision Connectors for 110 Ghz , EL

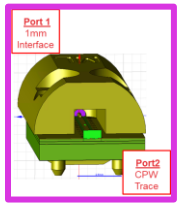
- Great performance to 120+ Ghz
- Located on the Edge of the PCB
- Hard to ensure PCB copper planes and traces go to the edge of the PCB (good return path), which may require PCB post-processing.

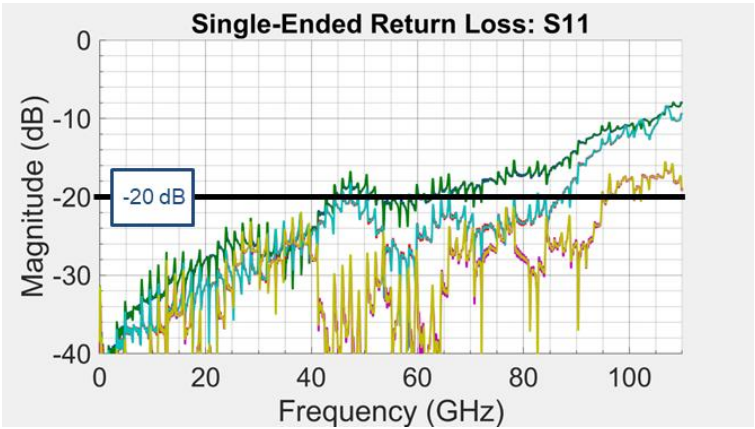


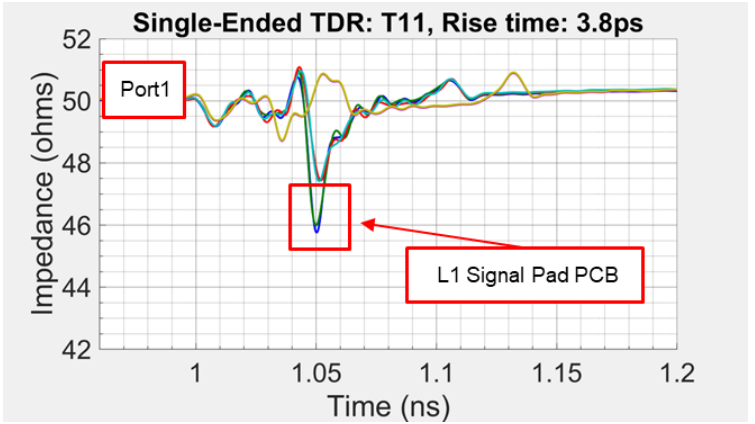
Precision Connectors for 110 Ghz , Summary

- Optimized Footprint (IL/RL) cascaded with:
  - 1inch and 1.5inch traces.
- Signal Pad Diameter: 12 mil / 0.3048mm

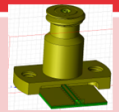
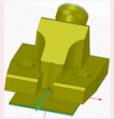
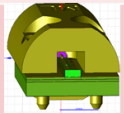


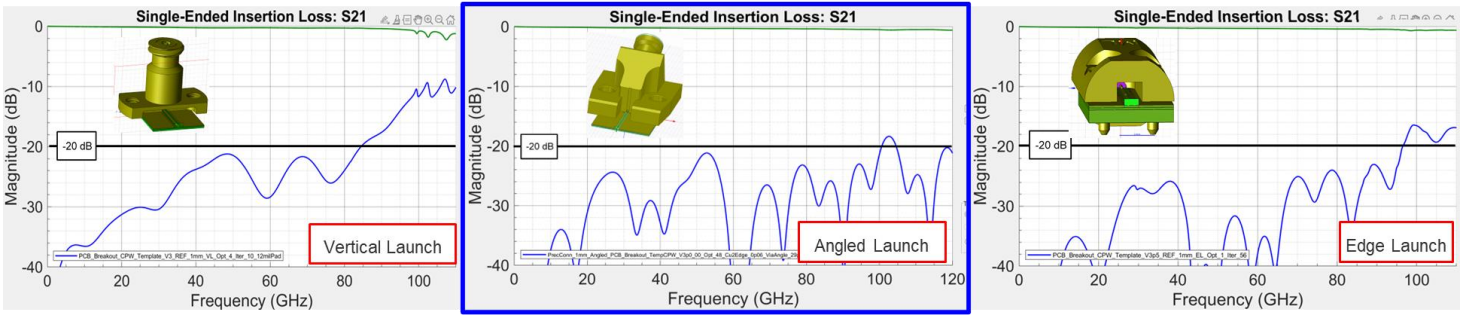






Interconnect 110 GHz Test Board Design

	Interconnect	Notes / Comments
Vertical Launch		• Solid Performance through ~90 Ghz • Placed anywhere on PCB • Readily available, small form factor (can place them close together)
Angled Launch (30 deg)		• Great performance to 120+ Ghz • Placed anywhere on PCB • “Standard” footprint can show excellent performance without pushing the manufacturing envelope.
Edge Launch		• Great performance to 120+ Ghz • Located on the Edge of the PCB • Hard to ensure PCB copper planes and traces go to the edge of the PCB (good return path), which may require PCB post-processing.



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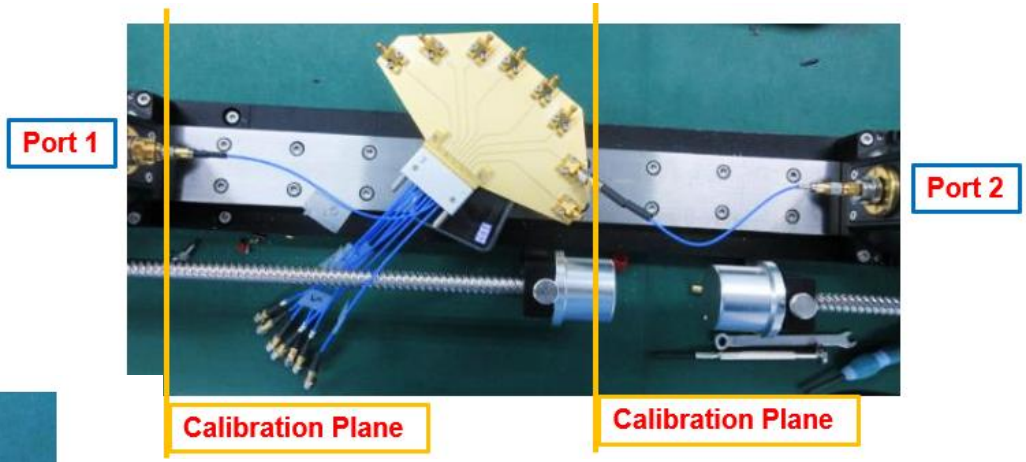
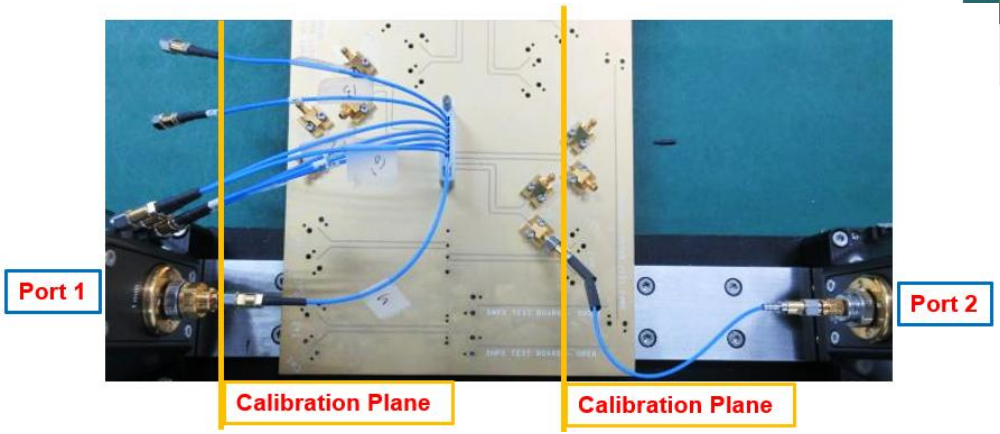
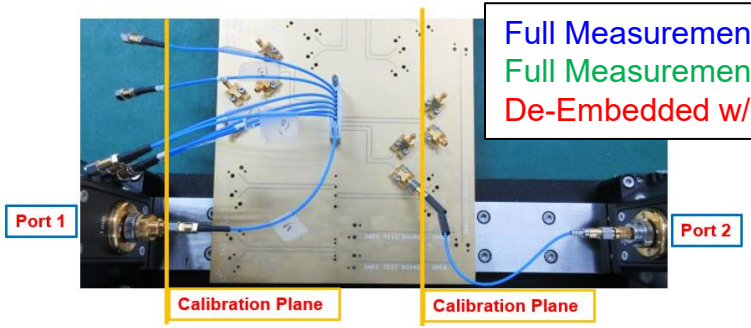
  - RF Interconnect Modeling & Validation
  - Precision Connectors
  - **Test Fixture Validation & Review**

Interconnect 110 GHz Test Board Design, Final Results

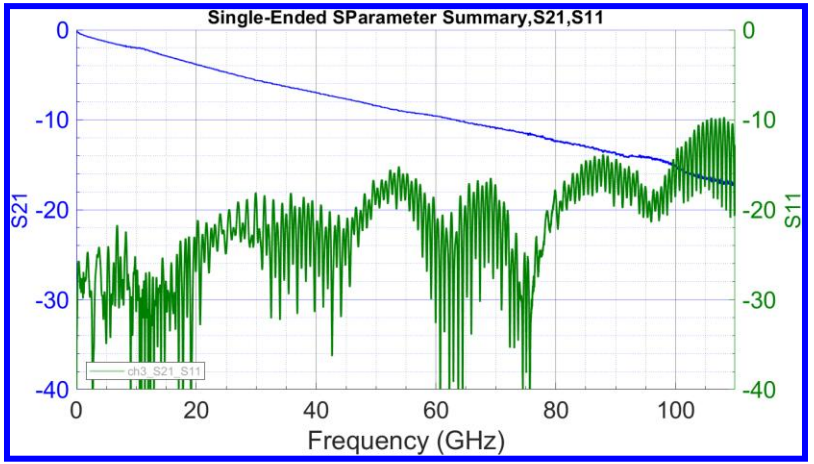


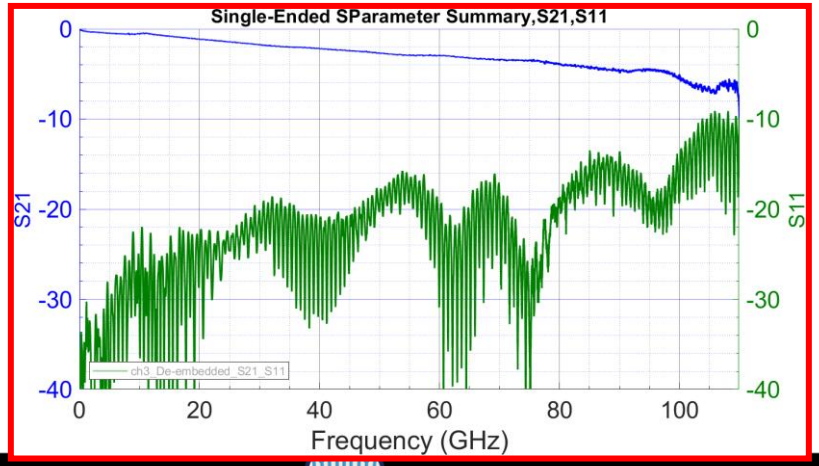


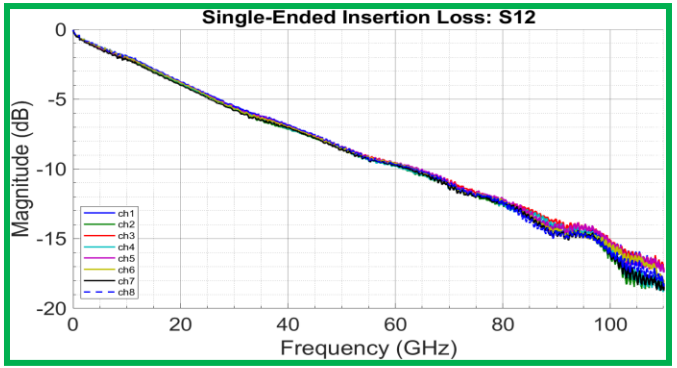
Interconnect 110 GHz Test Board Design, Final Results, VL



Full Measurement
Full Measurement, All Channels
De-Embedded w/ 2x Thru

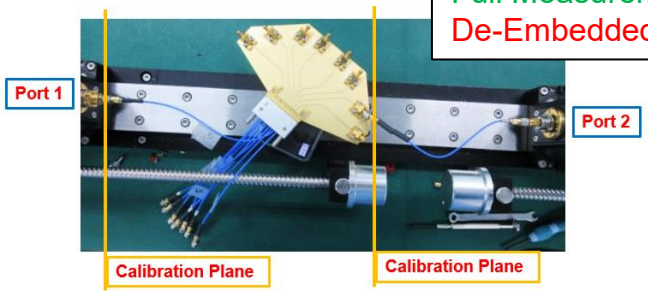


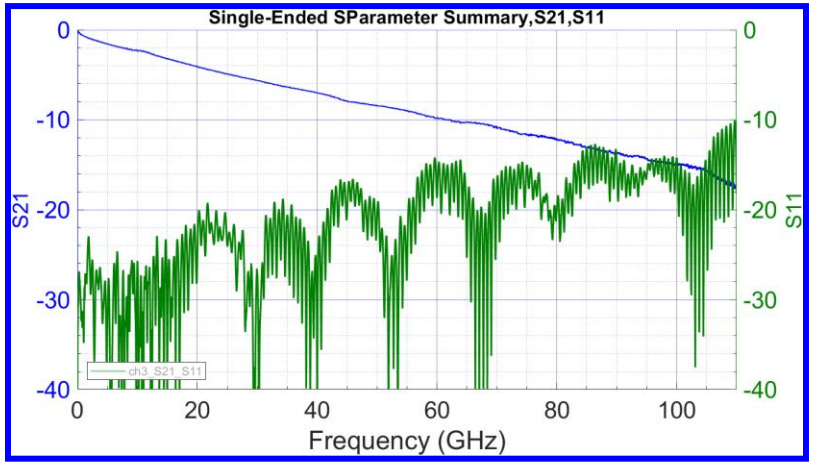


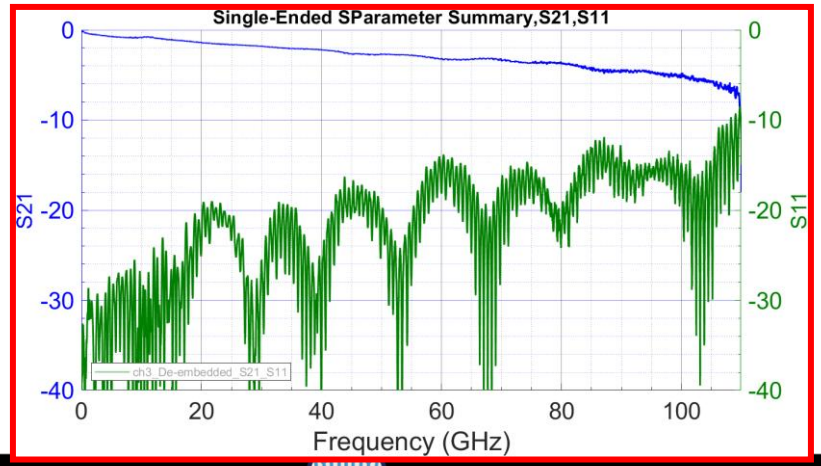


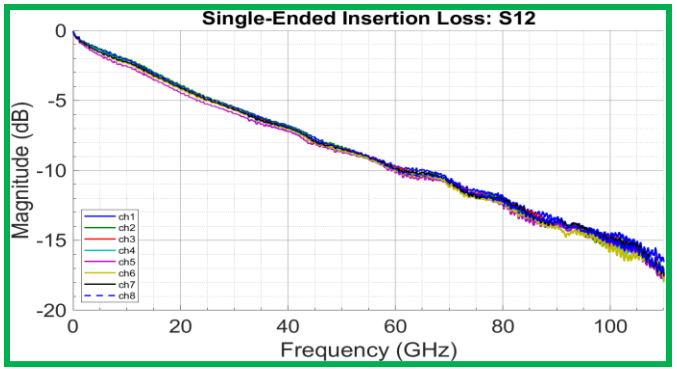
Interconnect 110 GHz Test Board Design, Final Results, EL

Full Measurement
Full Measurement, All Channels
De-Embedded w/ 2x Thru







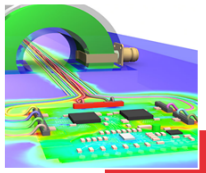


Summary

- Signal Integrity Production flow also requires tooling, fixtures to achieve consistency, scale, etc.
- Signal Integrity Tooling/ Fixture Design
  - Parametric Model of the interconnect and any mating assemblies (cable, PCB, other interconnect)
  - A parametric model is an abstract model than enables the rapid modification of geometry.
  - 3D Field Solver (accurate and reasonable runtime)
  - Validation of extracted performance vs. the target specification.
  - Consistent Material library, extraction settings (excitations, boundary conditions, etc.) and database of simulated data (SParameters)
- Artificial Intelligence/ Machine Learning (AI/ML)
  - Enables operator independent basic signal integrity production workflows
  - Limited/Constrained Solutions Space
  - Scaling of Engineering Resources

Manufacturing / Production

- **Manufacturing Process**
- **Input:**
  - Components/Assemblies
- **Validation:**
  - VNA, Optical Inspection
- **Output:**
  - Finished Interconnect and Cable Assemblies, Documentation
- **Production Fixtures/Equipment**
  - Laser Cut
  - Tinning
  - Solder Station
  - Hot Bar
  - Press fit Fixtures
  - Assembly Fixtures



Signal Integrity Workflow

- **Signal Integrity Workflow**
- **Input:**
  - 3D Component Models, Assembly Model (cable, PCB)
- **Validation:**
  - 3D Field Solver
- **Output:**
  - Optimized Interconnect and Cable Assemblies, Documentation
- **Production Fixtures/Equipment**
  - Parametric Models
  - Cascading Engine
  - High-Performance Computing Resources

Thank you!

QUESTIONS?

Raul Stavoli

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Raul.stavoli@Rosenbergerna.com | https://rna.rosenberger.com/