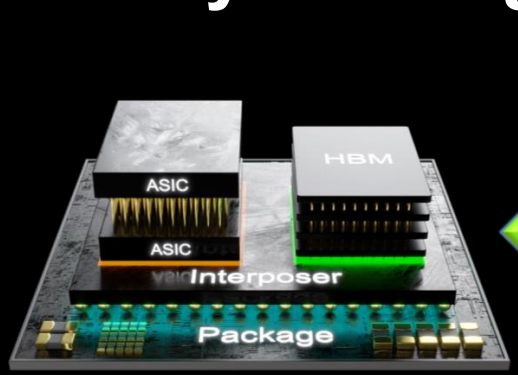
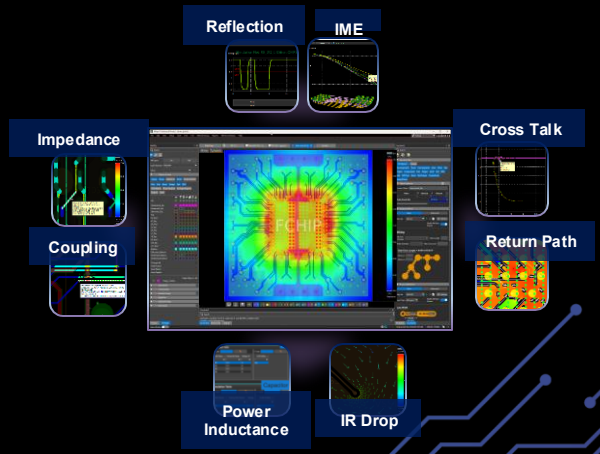
Tackling the Complexity of Next-Gen IC Packaging: System-Level Design and Analysis Insights





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SPEAKERS

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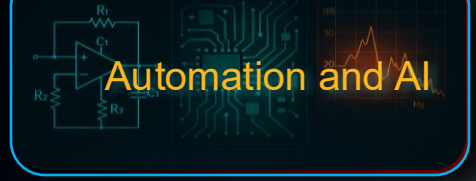
Bgriffin@cadence.com | cadence.com

Presentation Focus:

Multi-Fabric Layout

3D-IC Architecture



System Analysis

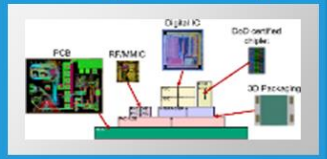
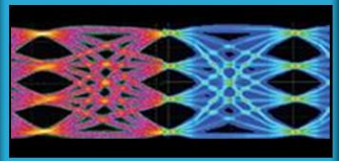
The Shift in IC Packaging

3D-IC vs 3D Packaging

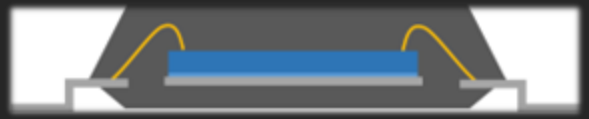
Layout Automation

Analysis and Signoff

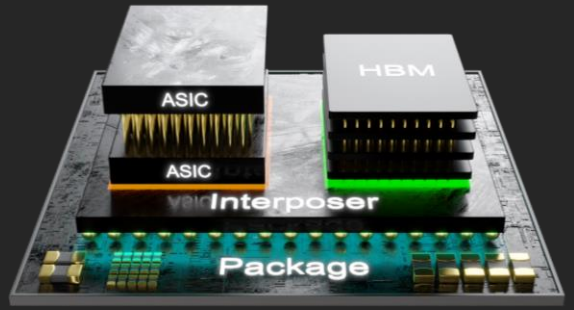
Major Electronics Industry Challenges and Cadence Solutions

Achieving PPA targets at advanced nodes	Chiplets, 3D packaging, and PCBs	High-frequency analog and RF design	IP to system-level optimization and analysis	System verification throughput and early development
Large chips, TTM pressures, expensive respins	Chiplet interoperability, meet PPA and thermal constraints	Performance and multiphysics interactions	System stack is a key opportunity to differentiate	Early software integration, system debug complexity
100s of 3nm tapeouts 2nm flow development Digital full flow 2000+ AI-driven tapeouts	 Chiplet and package co-design and analysis 	 RF/5G design and verification 	PCIe® 5.0/6.0 LPDDR6 High-Speed SerDes Interchip UCIe™ Enterprise IP and software stacks 	 High-capacity and performance hardware 
AI automation of digital full flow	PCB design and optimization	RF simulation, signal/power integrity	Scientific computing GPU acceleration	AI-optimized formal, simulation, and debug

Where We Have Come From…

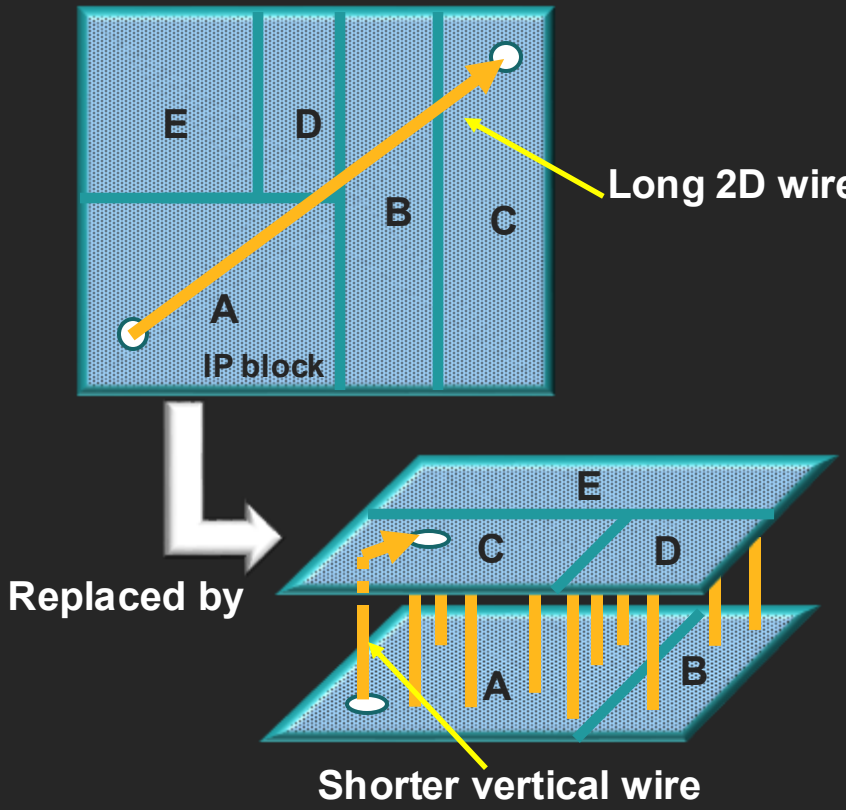


- Yesterday's advanced IC packaging was often considered a *necessary evil*
  - Avoid negative impact on chip
    - Electrical, thermal, mechanical
  - Protect chip from the outside world
  - Redistribute I/O to pitch more suitable for the PCB layout



- Today's advanced IC packaging *adding value*
  - Multi-chip(let) solutions leading the way for "More than Moore" vision
  - Companies leveraging packaging technologies to create value and differentiation from their competitors
  - TSV, WLP, and 3D stacking technologies providing a tremendous number of packaging options for all form factors

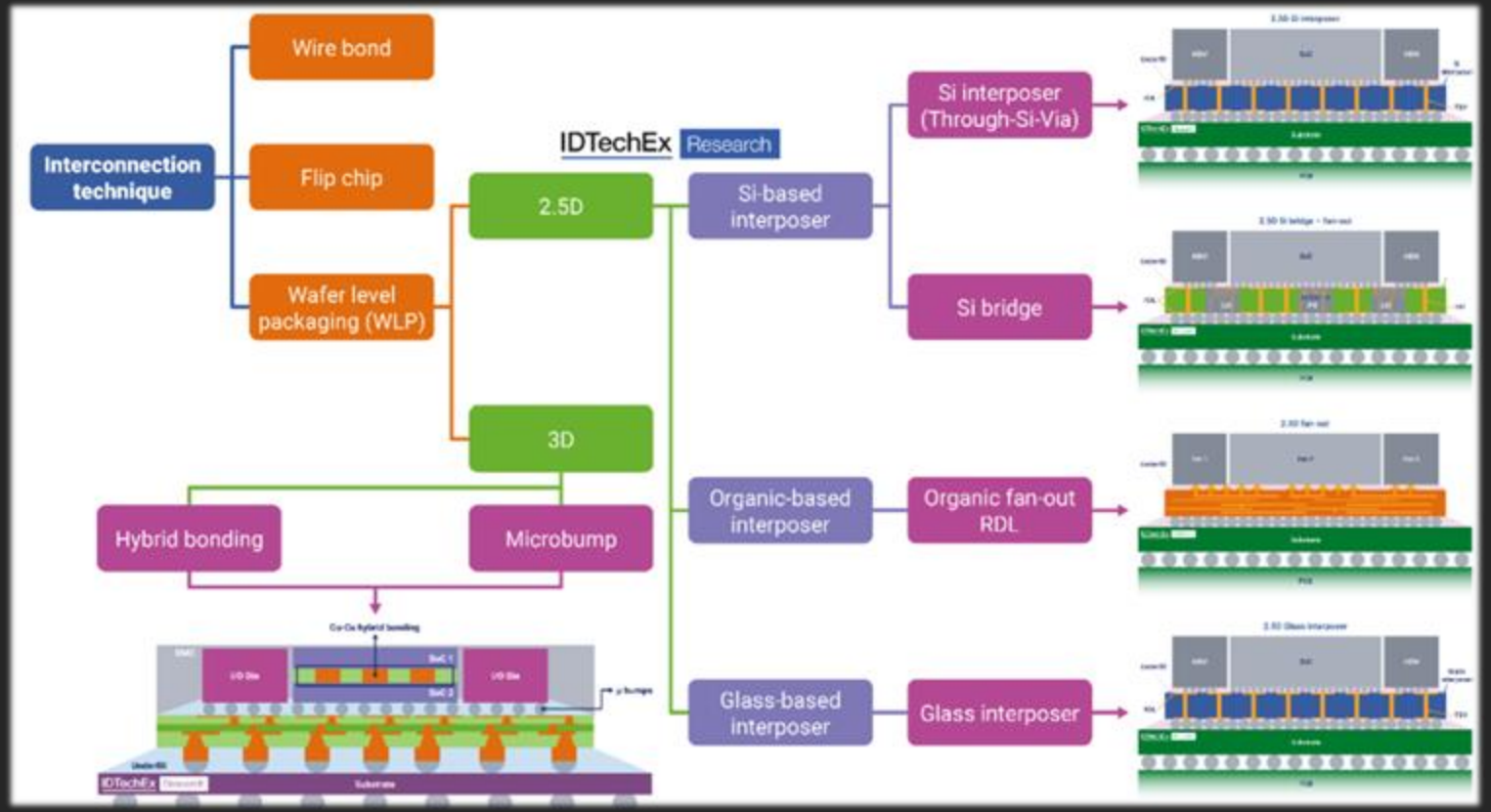
Common Example For 3D Die/Wafer Stacking



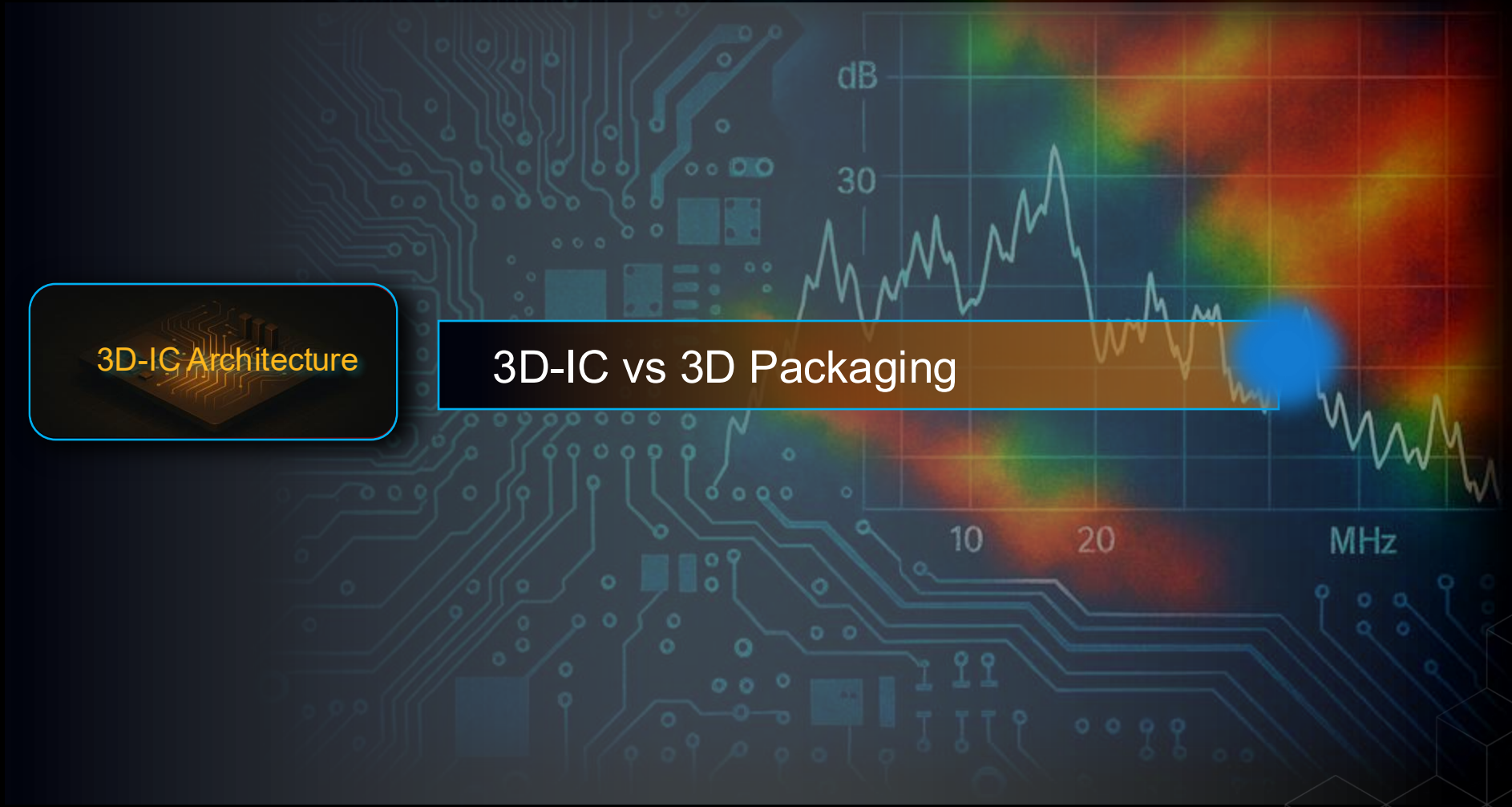
- Shorter Wire
- Less Power
- Higher Performance
- Higher Bandwidth
- Smaller Profile
- Better Yield

2.5D/3D Advanced Packaging and 3DIC Die Architecture

Advanced Package Structure Flow Chart



https://www.idtechex.com/en/research-report/advanced-semiconductor-packaging-2025-2035-forecasts-technologies-applications/1042



3D-IC Architecture

3D-IC vs 3D Packaging

3D Advanced Packaging and 3D-IC Architecture Summary

2D SOC to 3D-IC ARCHITECTURE

DIGITAL

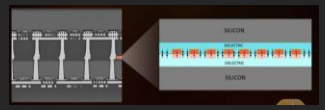
Vertical IP Integration

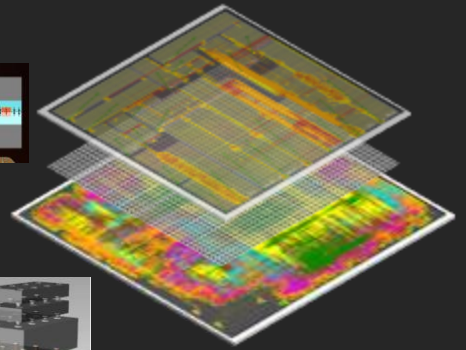
3D die stack digital architecture with IP-to-IP timing considerations

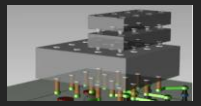
Single RTL partitioned at implementation - Full IC required for layout (TSV for vertical stack)

With solderless die-to-die interconnect (hybrid bonding)

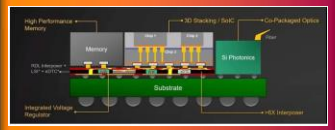
Creates 3D-IC Die stack block with a single output netlist







2D/3D/ADVANCED PACKAGING



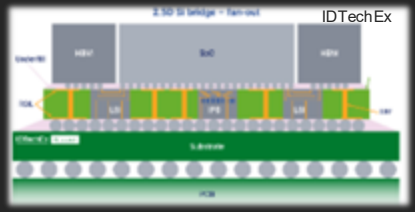
Single- or multi-ie (hetero/homogeneous integration)

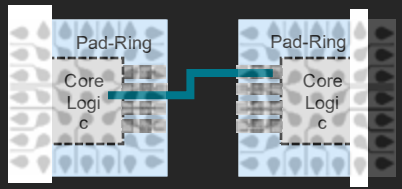
Dies designed independently- black box model

I/O buffer to I/O buffer and individual die ESD structures (BoW, UCIe, AMBA CHI, UMI, etc.)

Generally, solder-based die-to-die and die-to-substrate/RDL interconnects (Except for RDL/embedding or Chip First RDL)

Single or multi-plane/fabric die integration
Can integrate 3D-IC die block option (post block design)



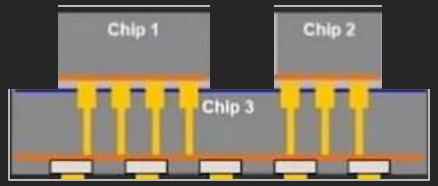


I/O buffer to I/O buffer
(BoW, UCIe, AMBA CHI, UMI, etc)

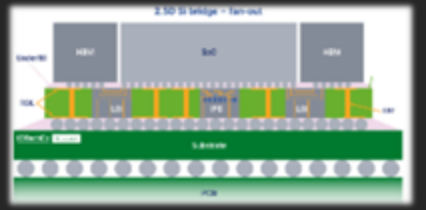
When to Consider 3D-IC and 2D/2.5D/3D Advanced Packaging

Drivers:

- ❑ Power/Bit
- ❑ Si Node Yield/Size/Cost
- ❑ Heterogeneous Integration
- ❑ PPA



3D-IC Architecture



2D/2.5D/3D Advanced Packaging

Feature	Copper-to-Copper (Hybrid Bonding)	Solder Interconnects (Microbumps)
Interconnect pitch	Very small (≤10 µm)	Larger (20–40 µm+)
Electrical resistance	Low	Higher
Parasitic inductance	Very low	Higher
Parasitic capacitance	Moderate/low	Higher (due to larger pad/UBM)
Signal bandwidth	Much higher	Limited at very high frequencies
Crosstalk	Lower (shorter paths, tighter geometry)	Higher
Eye-diagram quality at high speed	Superior	Weaker
Power delivery noise	Lower	Higher
Thermal behavior	Better	Worse

OpenAI

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Why Advanced Packaging Is the Market Driver - Value Wave

- **Structural Shift 1**: The package has become the system.
  - Bandwidth and energy targets now solved in the **interposer and stack,** which shifts performance bottlenecks into die-level assembly.

- **Structural Shift 2**: Front-end style process control is moving into packaging lines (focus of equipment vendors) Traditional flip-chip equipment vs fab-like processing (wafer-based)

Vishal Saroha-Yole Group 2025-WhitePaper

- **Design Shift**: Components of new Advanced Packaging System now must consider the multiphysics impacts on each other – Shift-Left Analysis. Database management by tools and automation critical.

Memory Block (Thermal, SI/PI)

3D-IC Design Block (Thermal, SI/PI, EMI)

Silicon, Mold/RDL, Glass (SI/PI, Warpage)

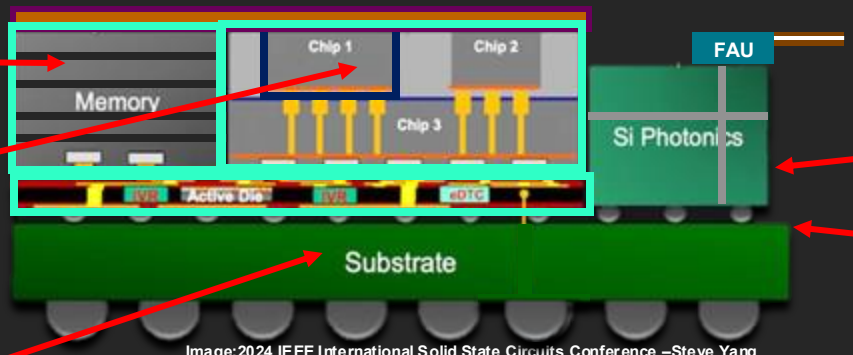


Image:2024 IEEE International Solid State Circuits Conference –Steve Yang

Substrate (SI/PI, Thermal, Warpage)

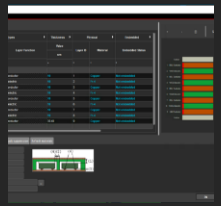
Optical Engine Block (Warpage, Thermal)

Package Level Die/Block Layout/Placement (SI/PI, Thermal, Warpage)

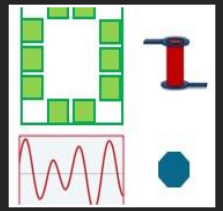
Key Challenges for New IC Package Structures

- Packages becoming larger and complexity/density increasing, which is driving longer design cycle times.
-
- Ability to create bridge die for dense connections between processors and memory with certified performance. Simple LSI bridge now more complex with DTC built in and TSVs.
- In-design analysis and shift-left design analysis more critical to better understanding system-level impact earlier in the design process. Eliminating exiting the layout tool for analysis during the design process.
- System-level die/component hierarchical planning and early analysis while also considering LVS/DRC.
- Physical verification with improvement to minimize DRC-related incidents.

TechFiles



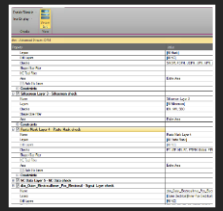
Design Libraries



Assembly Rules

Compliance Kits

Manufacturing Rules



Rule Decks

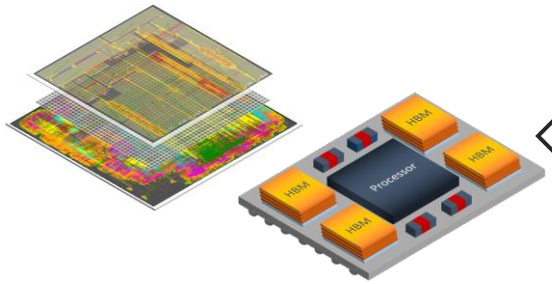
Integrity™ 3D-IC Platform

Integrity System Planner
(Top-level planning, optimization and early-stage analysis)

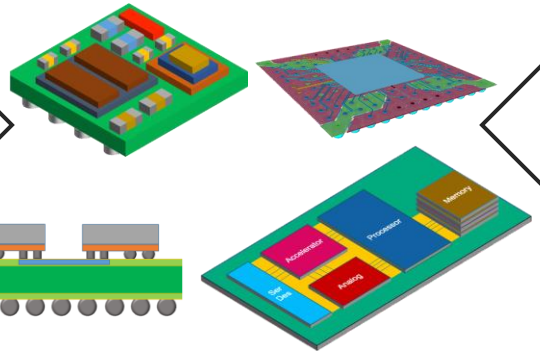
Virtuoso/AWR
(Analog/RF/Photonics)

Integrity 3D-IC

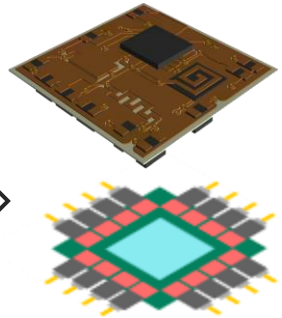
Allegro X APD



Co-Design



Co-Design



Allegro X (Integrity Option)

Allegro X (VMT)

Sigrity X, Clarity, Celsius, Voltus & Pegasus
(EMIR, 3D-EM, Signal Integrity, System Power/Thermal, DRC/LVS and SystemLVS Sign-Off)

Digital IC Designer

Primarily LINUX OS
Chip-on-wafer and wafer-on-wafer
Based on Innovus 3D-IC
Dies/Chiplet detailed editing level

Package Substrate Designer

Primarily MS Windows OS
Multi-die, multi-chiplet substrate layout
Die abstract editing level
3D-EM, signal Integrity, system power

RFIC Designer

Primarily LINUX OS
Targets RF module design
Integrated circuit simulation
Electromagnetics extraction

Allegro X APD Multi-Chiplet 3D Packaging Sub-Flow

Integrity™ System Planner
(Planning, optimization and early-stage analysis)

1

PVS/Pegasus™
(Physical Verification)

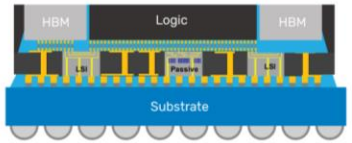
Allegro® X APD

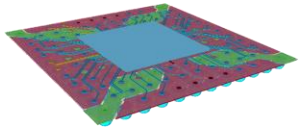
2

Silicon Layout Option

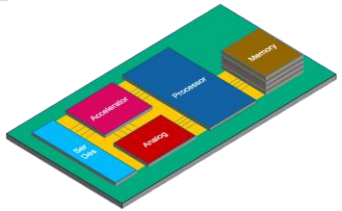
System-in-Package

2.5D with Bridge

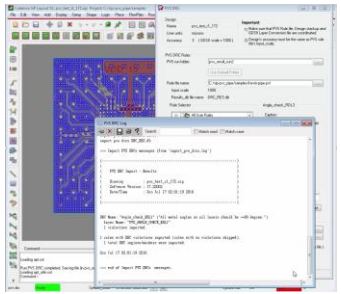




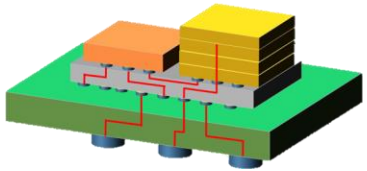
FOWLP



RDL Interposer



Signoff DRC



SystemLVS

Sigrity™ X (Aurora for IDA), Clarity™, Celsius™, Voltus™
(3DEM, Electrical and Thermal Signoff)

3

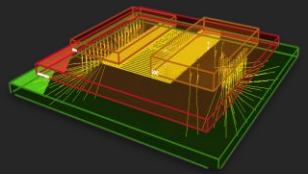
- Techfile-driven correct-by-construction layout
- Supports OSAT and foundry-based packaging technologies
- Flexible connectivity creation, including layout-driven design
- Automated library development
- Seamless 3DEM and thermal modeling integration
- In-design electrical analysis, DFA and DFM
- Co-design capabilities with Innovus™ and Virtuoso®

cadence

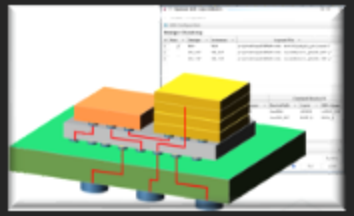
1 Integrity System Planner: Enabling a Robust Muti-Chiplet Flow

Multi-Fabric Signal Mapping

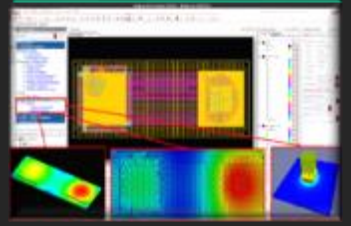
Hierarchical Planning / Connectivity Management



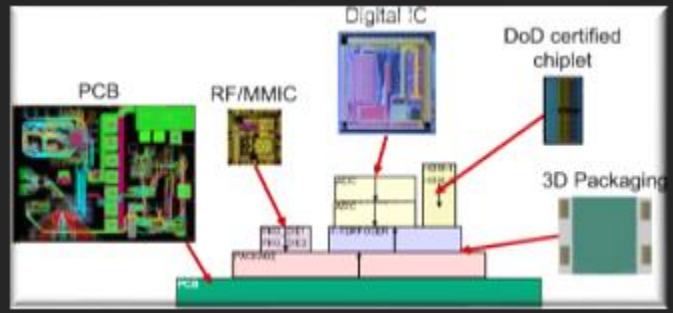
Stack Alignment / Verification



Early-Stage Multiphysics Simulation

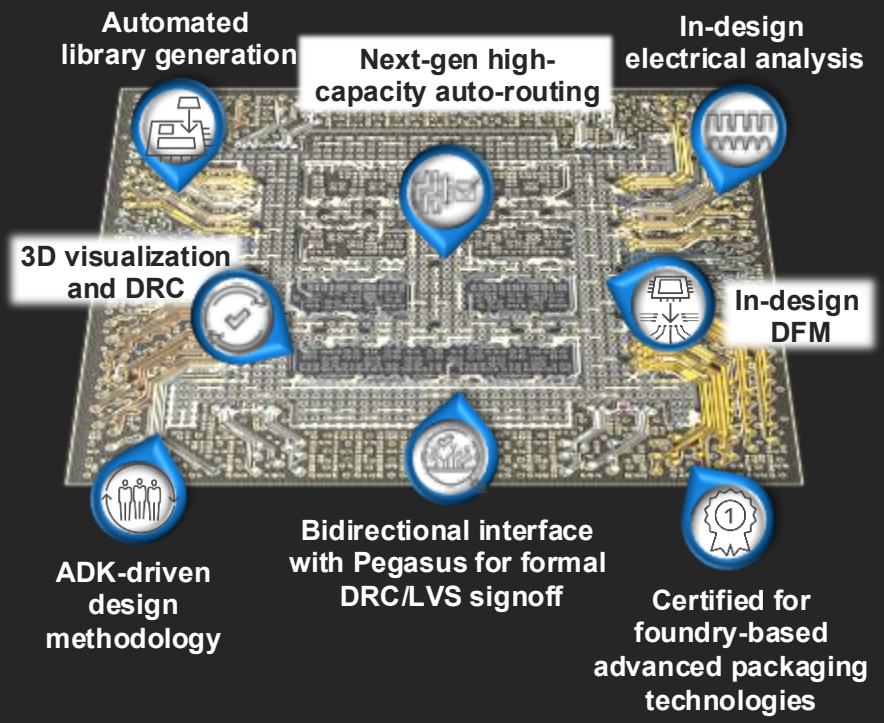


- Unified Design Environment
- System-Level Floorplanning
- Connectivity Optimization
- Early System-Level Analysis



Hierarchical Planning and Optimization of System-Level Design and Connectivity

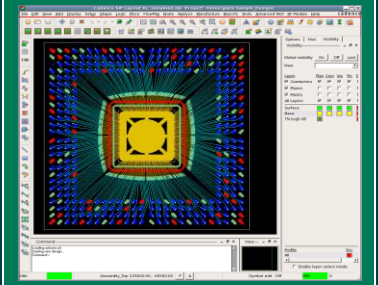
2 Allegro X Advanced Multi-Die Package Design Solution



- Industry-leading constraint-driven correct-by-construction layout with tech-file driven setup
- Advanced layout capabilities supporting in-design electrical analysis and DFM checking
- Multiple modes of connectivity creation, including layout-driven design
- Direct integration with Clarity™ and Celsius™ Solvers for seamless 3D-EM and thermal modeling
- Advanced co-design capabilities with Innovus™ (digital IC) and Virtuoso® (analog/RF IC)

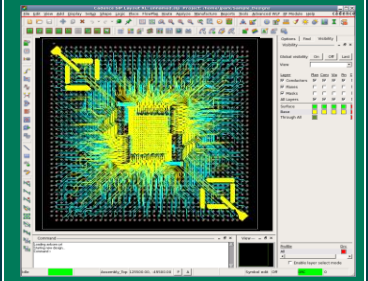
Allegro X APD- Advanced Multi-Die/Chiplet Packaging

Wirebonded PBGA



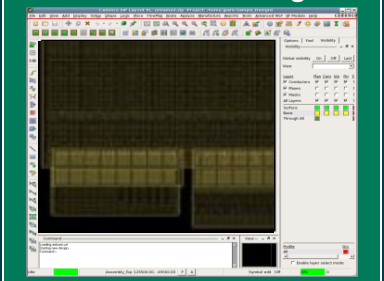
2D and 3D DRC checking
All-angle/radial routing

Flip-Chip BGA



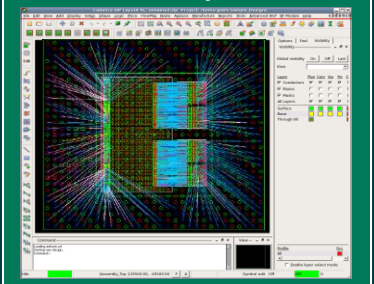
High-capacity
HDI structures and routing

Interconnect Bridges



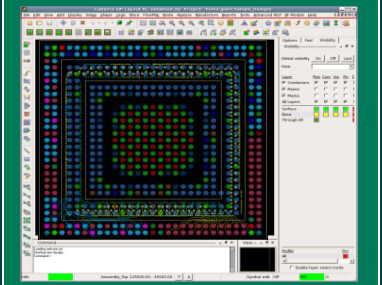
Embedded or elevated
silicon bridges

RDL Interposers



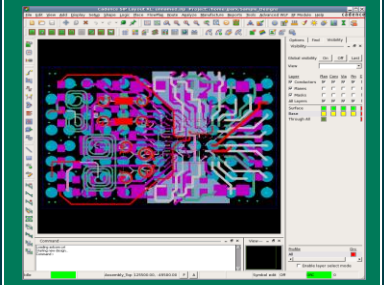
Ultra-high-density
HBM integration

Package-on-Package



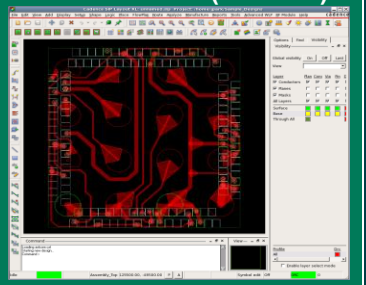
3D visualization and DRC
Auto signal assignment

RF Module



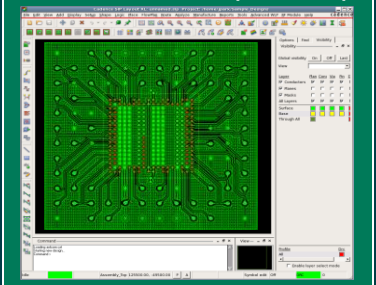
Virtuoso® integration
Parametrized structures

Fan-in WLP (WLCSP)



Merged IC and package layout
GDSII output

Fan-Out WLP (FOWLP)

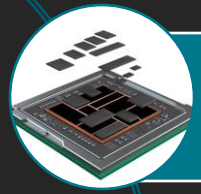


Integration with physical
verification tools

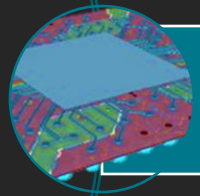
Allegro X AI Advanced Substrate Router (ASR)

Automated routing solution for multi-chiplet

Technology Rules

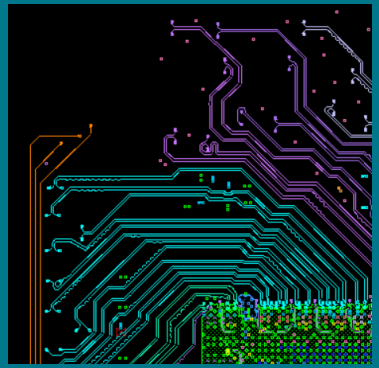


Optimized for routing high-density single-chip and multi-chip designs



Auto routes die-to-die and die-to-substrate connections

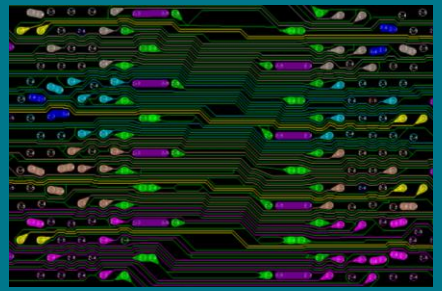
Multi-threaded engine enables significant performance boost



Die-to-Substrate Auto Routing

Auto-Routing for RDL/Substrate Layouts

Die-to-Die Auto Routing



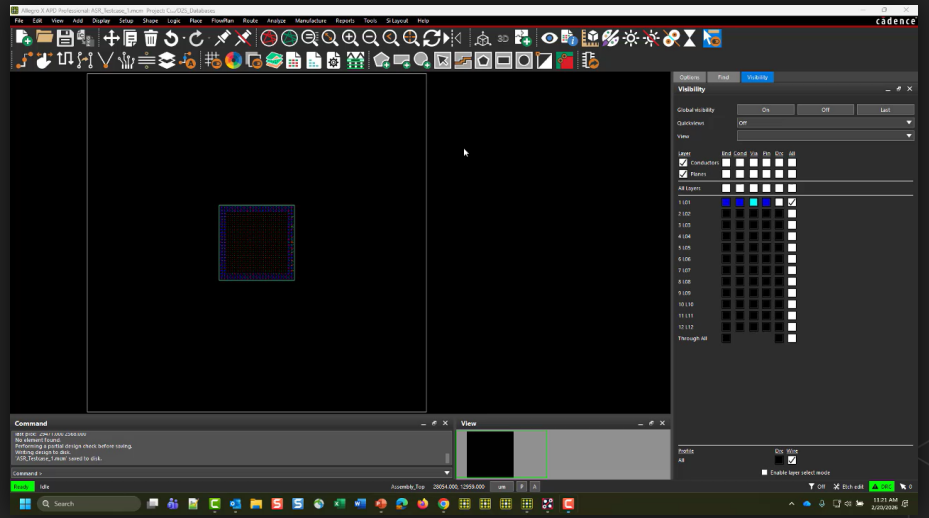
Advanced Substrate Router (ASR)
For IC packaging

- Bottleneck for advanced package design is ROUTING

- Optimized for routing high-density die-to-die and die-die-to-substrate connections, multicore performance benefits
  - 9 die D2S/D2D design takes ~55 min (4 cores)

- Supports diverse requirements
  - Any angle routing, auto shielding, bus breakout routing
  - High-density bump escape planning, differential pair routing
  - Fillet/teardrop insertion for yield improvement

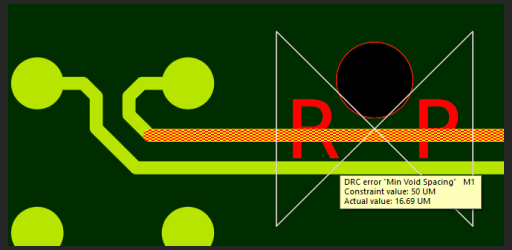
- Featured at foundry conferences
  - Endorsed by major foundries
  - Joint presentations with multiple semiconductor companies (Value Examples)



In-Design Analysis

3 Allegro X Package-Level In-Design Analysis

- Enables “shift-left” methodology by enabling issue identification and fixes right in Allegro X PCB and APD
- Package layout, tightly integrated with Clarity™, Celsius™, and Sigrity™ X technologies, enabling analysis directly from APD
- Multi-threaded to accelerate
  - **Impedance**
  - **Coupling and crosstalk**
  - **IR drop and power inductance**
  - **Reflection**
  - **Return path**
  - **Topology extraction**



Simulation Table

Single Ended | Diff Pair

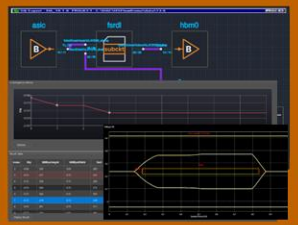
Summary Table

Net Name	Vias	No Ref	Impedance(Ohm) Max	Min	Typ	Impedance Length(%) Max	Min	Typ	Trace Total Length	Delay(ns)
PP_CLK0	3	0	83.30	74.50	76.30	0.23	5.81	87.28	4059.3520	0.640
PP_CLK0_N	3	0	83.30	74.50	76.30	0.23	5.81	87.28	4056.9430	0.640
PP_CLK1	3	0	98.20	74.50	76.30	0.08	4.70	86.02	4060.0050	0.641
PP_CLK1_N	3	0	98.20	74.50	76.30	0.08	4.70	86.02	4060.0130	0.641
PP_CLK2	3	0	100.10	74.50	76.00	0.61	4.41	82.99	4955.5290	0.785
PP_CLK2_N	3	0	100.10	74.50	76.00	0.61	4.41	82.99	4956.1590	0.785
PP_CLK3	3	0	84.10	74.50	76.00	4.88	8.85	79.93	4957.9040	0.783

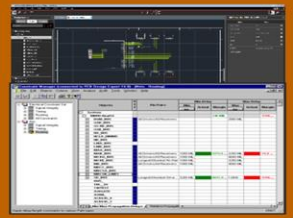
Detailed Table

Imp(Ohm)	Length	Trace Delay(ps)	Layer	Location (x;y)
74.50	2.6890	0.40	TOP	(3179.0277 200.8301), (3180.9289 198.9289)
98.20	3.2130	0.50	LAY4-SIG2	(292.0000 29.7473), (292.0000 32.9600)
76.30	12.7280	2.00	LAY4-SIG2	(3419.0000 157.0000), (3428.0000 148.0000)
76.30	16.9490	2.70	LAY4-SIG2	(292.0000 2.1422), (303.9847 -9.8425)
76.30	19.4800	3.10	LAY4-SIG2	(292.0000 2.1422), (292.0000 21.6223)
76.30	20.0000	3.20	LAY4-SIG2	(2788.7307 -172.2693), (2808.7307 -172.2693)
76.30	21.0000	3.30	LAY4-SIG2	(3398.0000 157.0000), (3419.0000 157.0000)
74.50	25.5560	3.90	TOP	(3228.8301 196.0000), (3246.9012 177.9289)
80.20	30.3150	4.50	TOP	(3390.0000 130.0000), (3420.3150 130.0000)

Exploration:
Derive Design Rules & Topologies

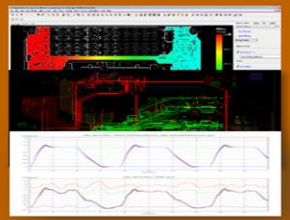


Implementation:
Schematic Entry & Constraint Assignment

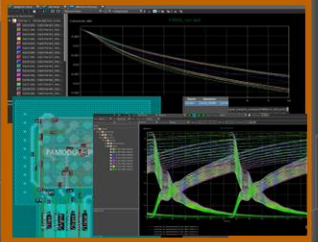


Constraint Driven Placement & Routing

In Design Analysis

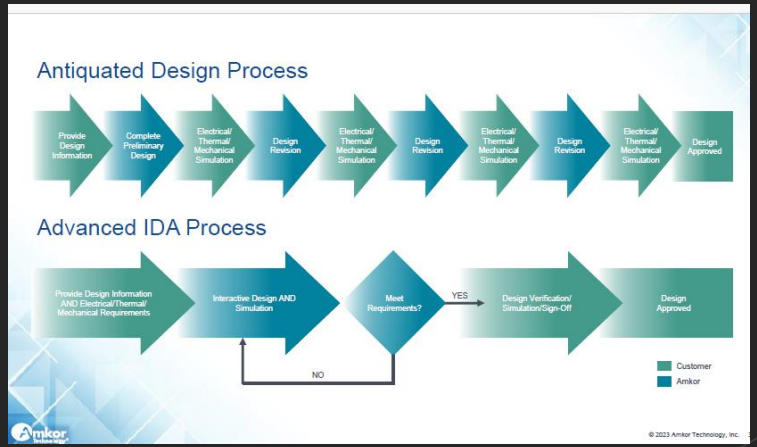


Post Route Verification and Compliance Signoff



In-Design Analysis Success

- VP of the R&D Design Center at Amkor
  - Implementing in-design analysis requires a mind shift
    - Designers do not instinctively want to perform analysis
    - SI/PI experts do not instinctively want to share simulation responsibilities
  - Because we have limited SI/PI experts, we must use shift-left analysis in the design cycle flow
  - The results:



Addressing Design Size Challenges with HGI Packages

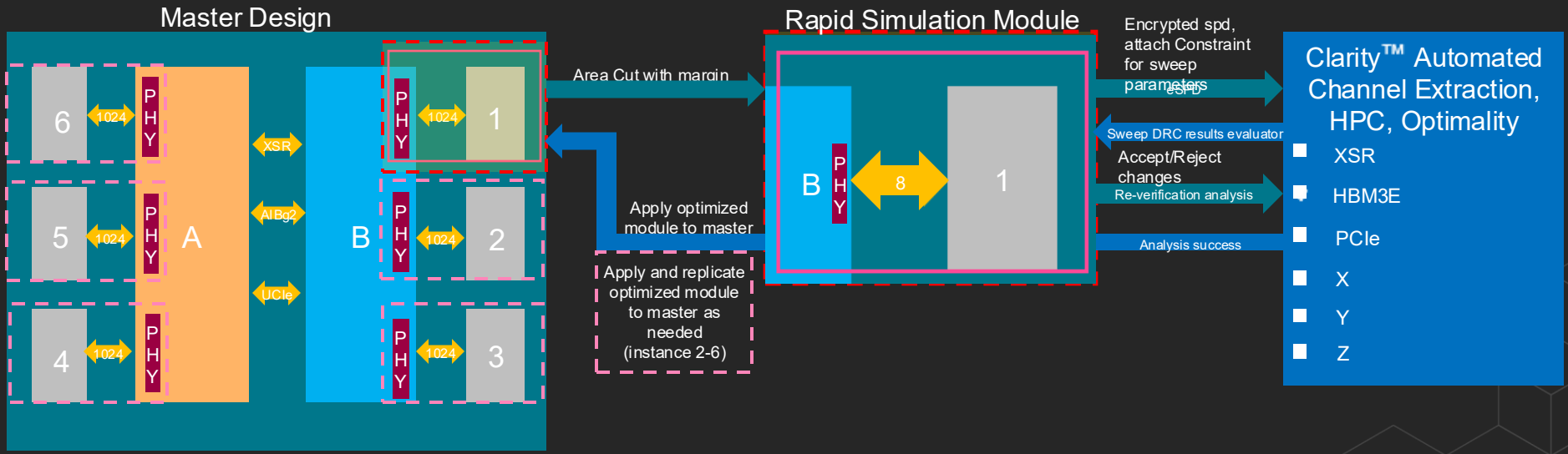
Problem

Customers cannot wait until the design is complete to simulate

Customers cannot dedicate hours / days to translate their designs into simulation tools

Solution: Algorithmic Selective Cutting

Shift SI and PI analysis left by focusing on a piece of the design

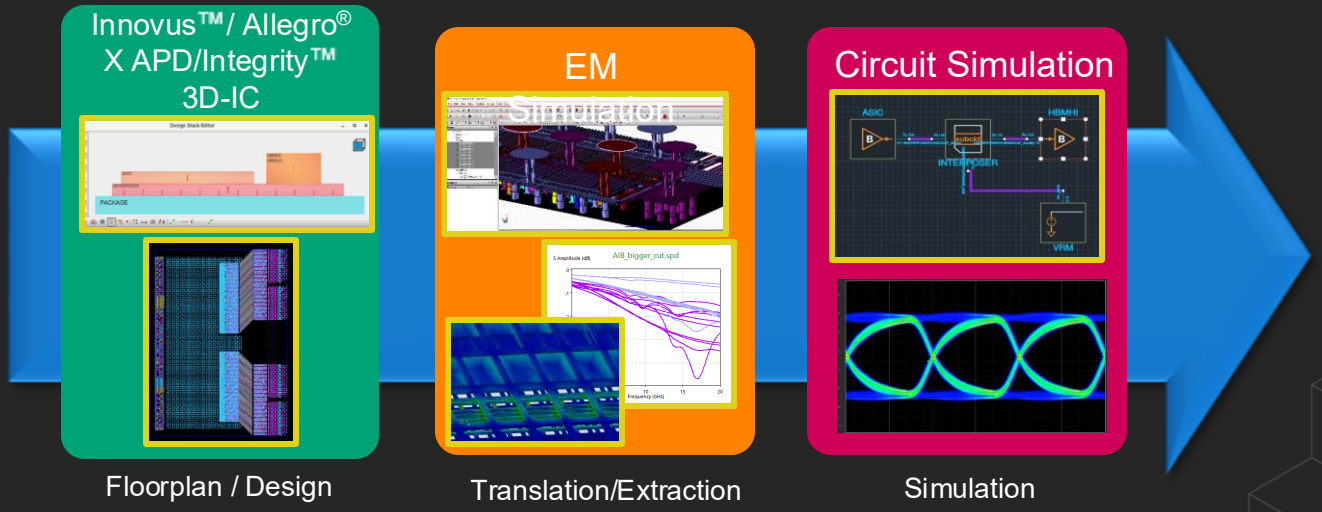


Addressing Challenges of Advanced Package Design Flow

- Translators and layout tools cannot scale linearly to address the growing scale of engineering designs
- Need to provide design teams the ability to distribute the layout and analysis efficiently within scalable workflows
- **Parallelization**, **integration,** and **TAT** are keys to success
  - Need to better integrate the layout of interposers, IC packages, and PCBs within the simulation and analysis domain (**multi-fabric analysis**)
    - More extractions needed and earlier in the design cycle

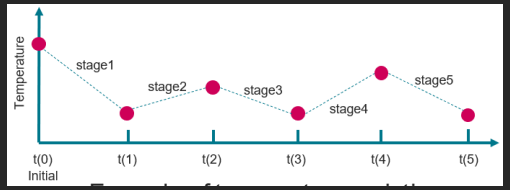
- **Hours spent** on large complex design translation from .gds to .spd
- After translation, trace/bumps become shapes. **Disabling** parameterization and optimization.

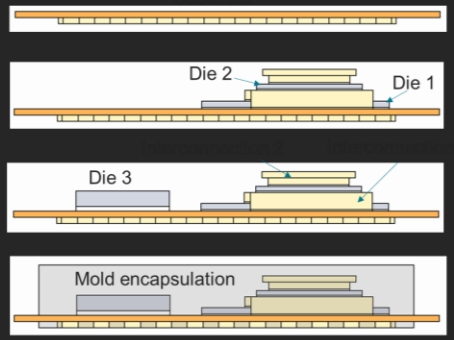
- **Redundant efforts** of selecting and cutting nets, generating ports.
- **Manual** topology setup and connection in time-domain

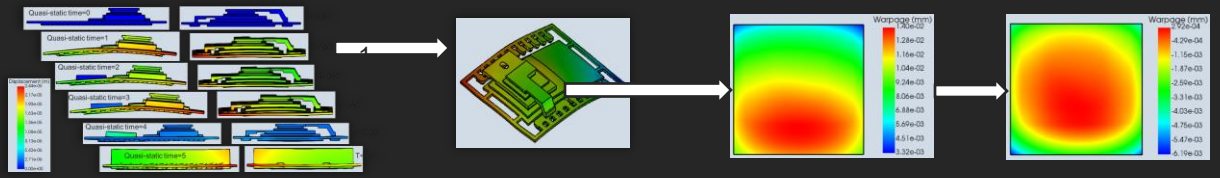


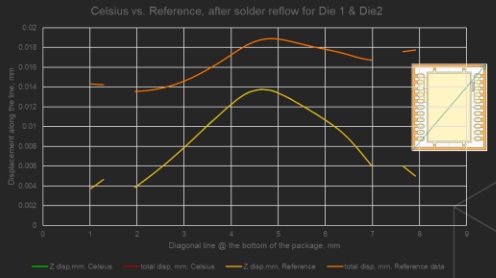
Celsius Warpage Analysis

- Warpage simulation for packaging process
  - Material and process
    - Thermal mismatch, temperature-dependent mechanical properties
    - Interconnection formation and mold encapsulation
  - Celsius™ Thermal Solver benefits
    - Look into warpage evolution for entire assembly process and figure out what process stage is at critical path
    - Suitable as a signoff for package design
    - Provides insights for assembly process engineer on process control



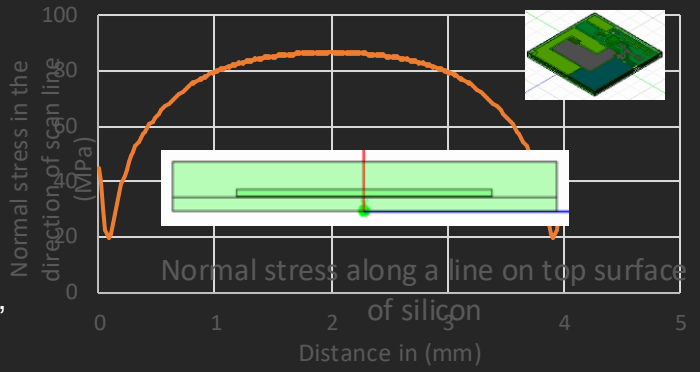


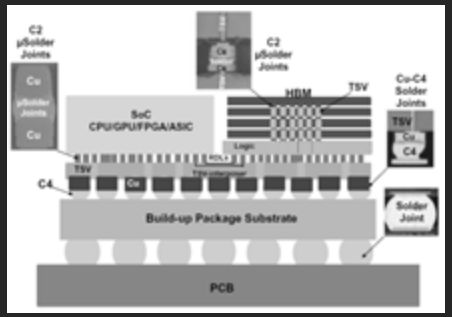




Celsius Stress Analysis

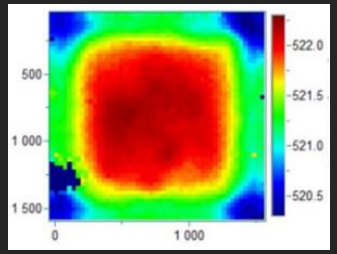
- Features in advanced package
  - Silicon active area, ultra-thin die, TSV
  - Cu RDL, passivation, polyimide stress buffer
  - Micron bumps, solder ball, solder cap, underfill, epoxy
- Global modeling
  - View overall deformation and stress field using simplified geometry, layer, and material properties
  - Leads to location high-deformation gradient and potential high stress spots, high-risk area for potential delamination, cracking, interconnection damage, etc.





Generate quadratic elements with default smooth transition, so user does not need to set many parameters before it can generate satisfactory meshes for analysis.

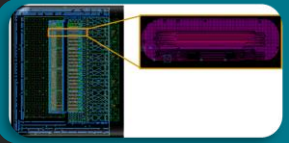
Celsius™ Thermal Solver has the following functions to assist in data analysis: (1) plot over line (2) plot all tensor stress components (3) plot other derived stress components in 3D canvas



Experimental measured bi-axial stress (MPa), showing very high level of silicon exists in semiconductor

Heterogeneous System Extractions

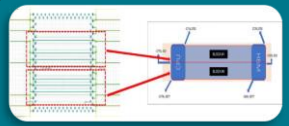
Multi-fabric analysis of interposers, IC packages, and PCBs



Interposer/PKG Design Cropping

- Group Relevant Nets and Areas for SI/PI Analysis
- Define cutting regions and margin
- Crop layout as desired with output .mcm, etc.

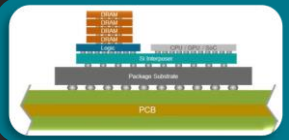
Cropping



Translation of target analysis nets and area

- Translate already cropped GDS/MCM/SIP files
- Model cleanup and translation for SIPI Analysis
- **Vastly reduced translation runtime and allows for easy sharing of IP blocks for SIPI analysis**

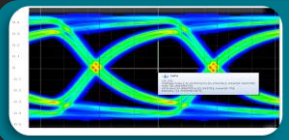
Translation



Interposer/PKG automated channel extraction

- Batch mode extraction of nets
- Define common ports, extraction setup
- **Traceability: Consistent results and enables easy comparison to previous Tapeouts or design iterations**

Automation



Verification of System Performance w/ Spectre

- Channel analysis with SystemSI

Verification

Optimization/Monte Carlo/Statistical Analysis: via translations, decap placement, routing, etc.

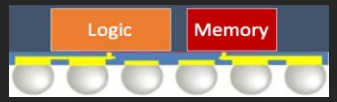
- Reduce to smaller .spd files for deeper analysis and to reduce runtime
- Provide constraints and run in Optimality
- Pass back constraints to Layout Designers for review

Optimization

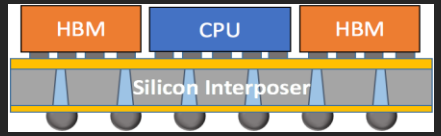
Signoff

Advanced IC Package Signal Integrity Analysis and Signoff

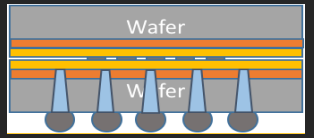
2.5D InFO



2.5D CoWoS



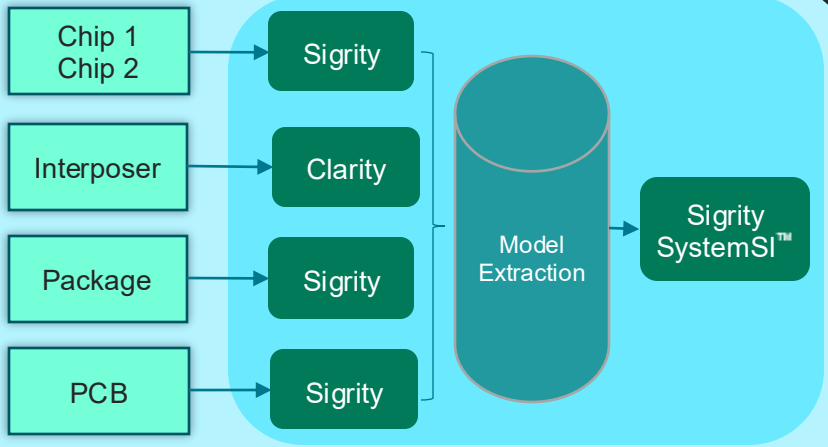
3D-IC *Wafer Stacking*



Package Extraction
Sigrity™ X

Interposer Extraction
Clarity™ 3D Solver

PCB Extraction
Clarity 3D Solver

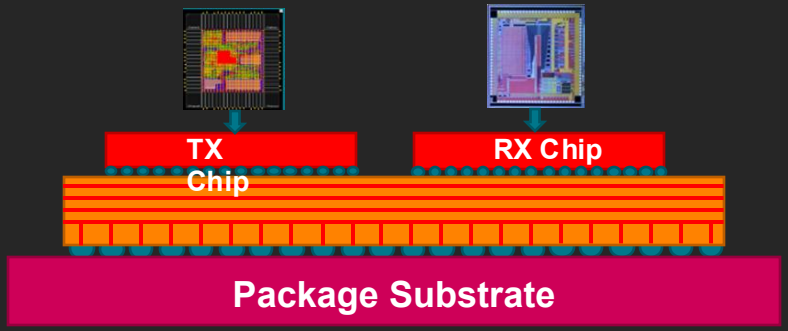


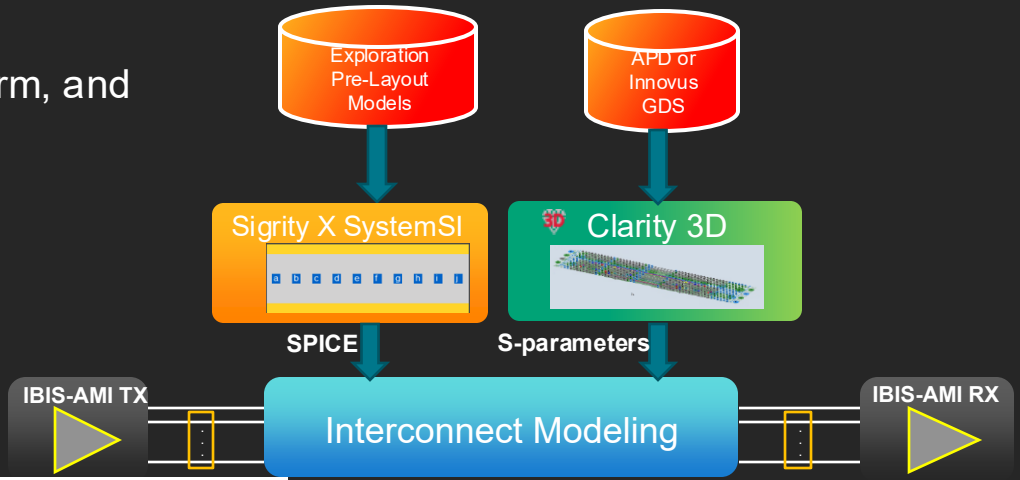
Build System-Level Simulations and Signoff

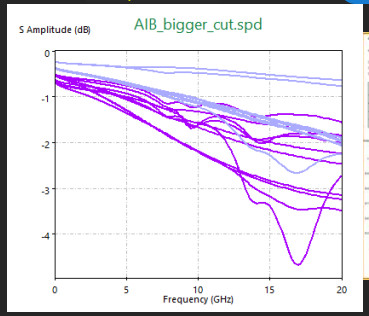
Model Extraction Using Clarity/Sigrity Technologies
Simultaneous Switching Noise Analysis
Power Noise Analysis

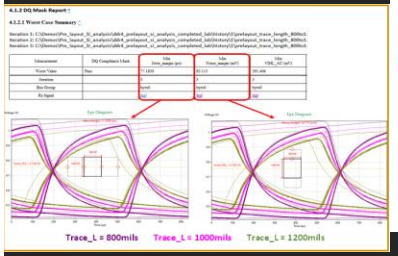
Signal Integrity Signoff Flow for Heterogeneous Integration

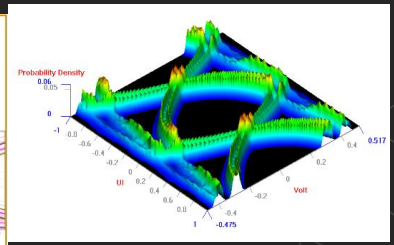
- Three platforms to cover full flow
  - Allegro® X Platform, Sigrity™ X Platform, and Clarity™ 3D Solver
- Exploration, in-design, and signoff
- Spec-driven compliance reports
- Analysis are scalable with core count





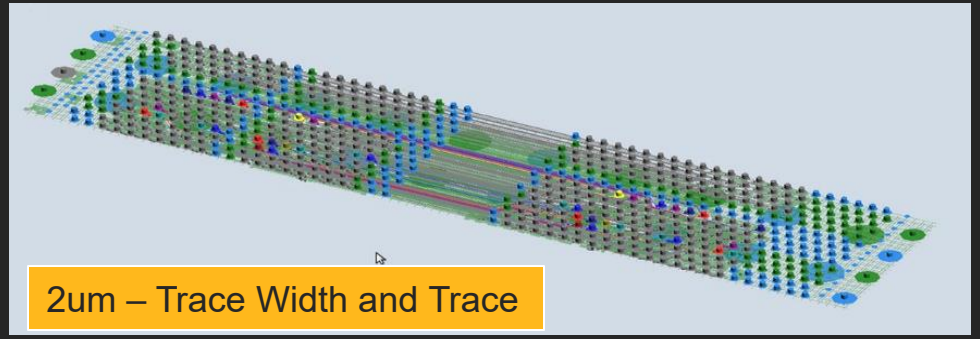


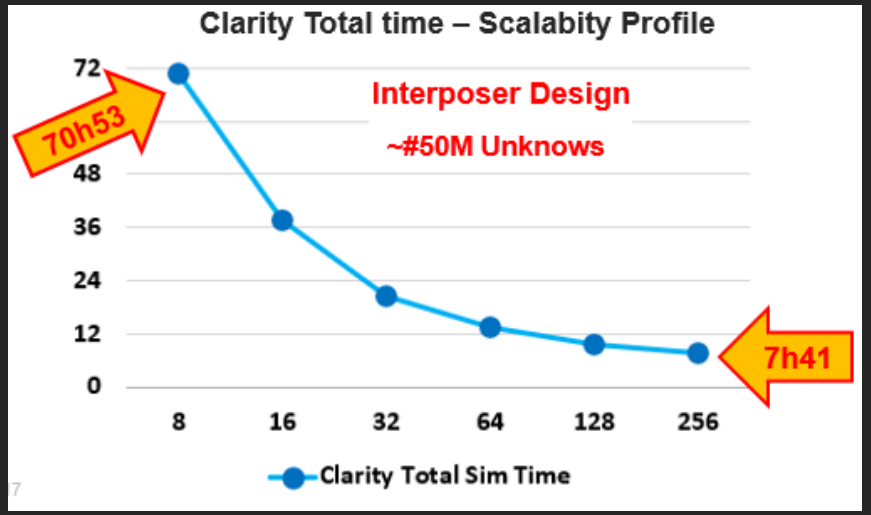


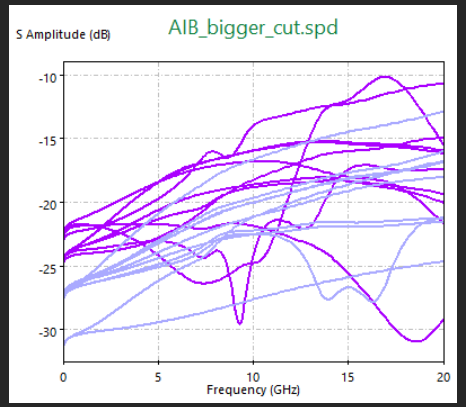


Case Study - Full 3D Extraction of Interposer with Clarity 3D Solver

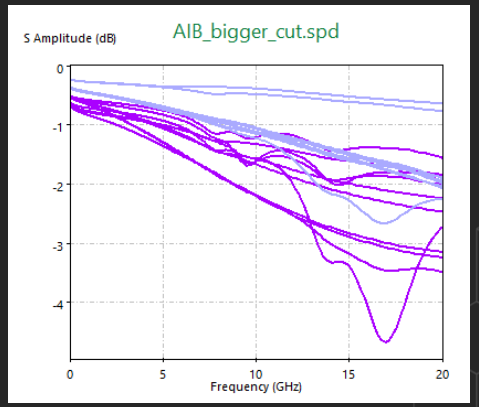
- 8-layer silicon interposer fully degassed
- 43 ports - 2 Byte Lanes + CLK signals
- Total Sim Time: 8 hours (256 Cores)
- Full 3D extraction scalable by core count







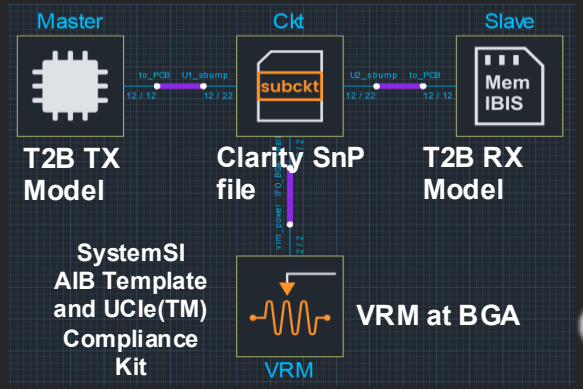
Byte Lane + CLK - RL

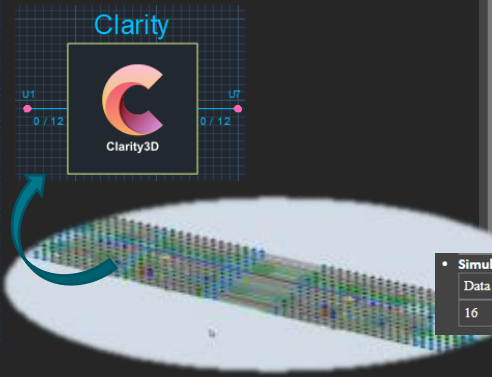


Byte Lane + CLK - IL

Sigrity X SystemSI Simulation Results with Interposer Model

- Public template for AIB topology
- Supports SPICE or IBIS-AMI from T2B
- Multiple interconnect types
  - Pre-layout, S-parameters, SPICE ckt, Clarity™ layout block
- Parametric sweep and optimization available
  - Geometric and AMI parameters can be swept
- Spec-driven Compliance Report – 6.4Gbps





2D Curves | Eye Density | Channel Report

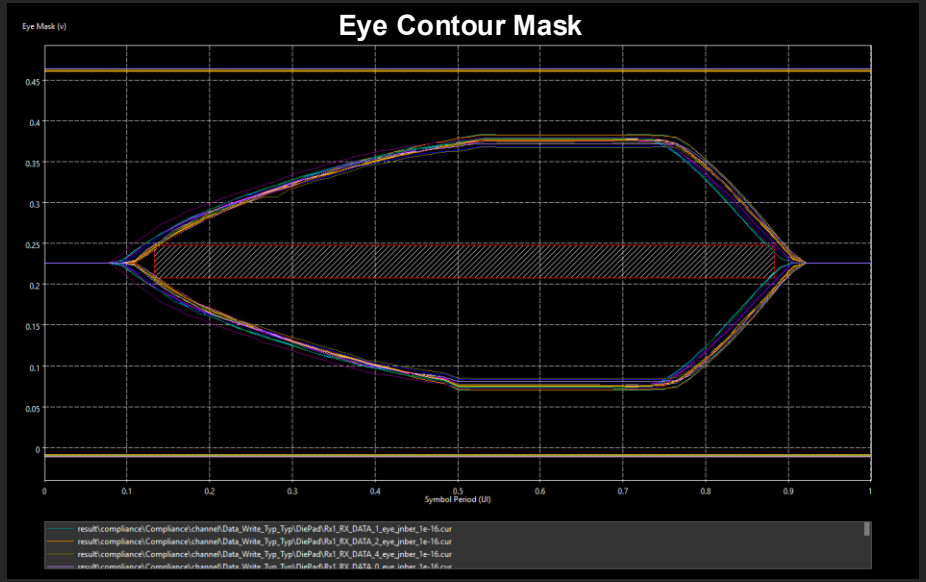
```
General:

        Simulation Type          = Time Domain
        Data Rate                = 6.4 Gbps
        Number of Bits           = 252416
        Number of Eye Bits       = 250824
        Ignore Bits              = 1592
        Channel Coding           = No
        Primary Driver           = Master_data0
        Data Pattern             = random
        Number of signals in bus = 10
        Characterization Data    = C:\Users\shawnm\Documents\shawnm\Internal\AIB\RAK_DB_SystemSI_AIB\result\1\Data_Write_Typ_Typ\DiePad\Char\Slave_data0.cur
        Characterization Type    = Even Mode Ramp Characterization


Jitter Inputs:

        Random Jitter            = 2 %

Noise Inputs:

        Random Noise             = 2 mV

Eye Contour Measurements:

        Eye Height               = 328 mV
        Eye Height Measured at   = 0.5 UI
        Eye Jitter               = 0.03 UI
        Eye Jitter Measured at   = 198 mV
        Eye Norm Jitter and Noise (NJN) = 0.42
        Channel Operating Margin (COM) = 33.44 dB

Eye Density Signal to Noise Ratio (SNR) = 83.92

BER Measurements:

        LBER(log BER)            Eye Width(UI)
        -21                      0.57
        -20                      0.58
        -19                      0.59
        -18                      0.60
        -17                      0.61
        -16                      0.62
        -15                      0.63
        -14                      0.65
        -13                      0.66
        -12                      0.67
        -11                      0.69
        -10                      0.70
        -9                       0.72
        -8                       0.73
        -7                       0.75
        -6                       0.77
```

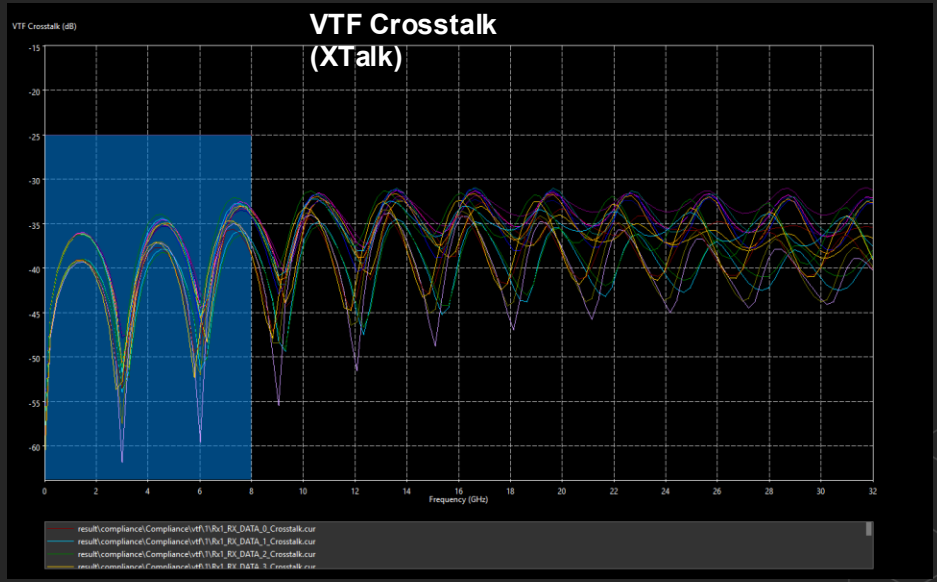
- **Simulation Properties:**

Data Rate (Gbps)	Log BERs	Ignore Time (ns)	Minimum # of Bits	Bit Sampling Rate	Log BER Floor
16	-16	200	10000	64	-15

Sigrity X SystemSI Eye Mask and VTF XTalk Simulation Results

- Easily check and verify eye contour with mask
- VTF crosstalk

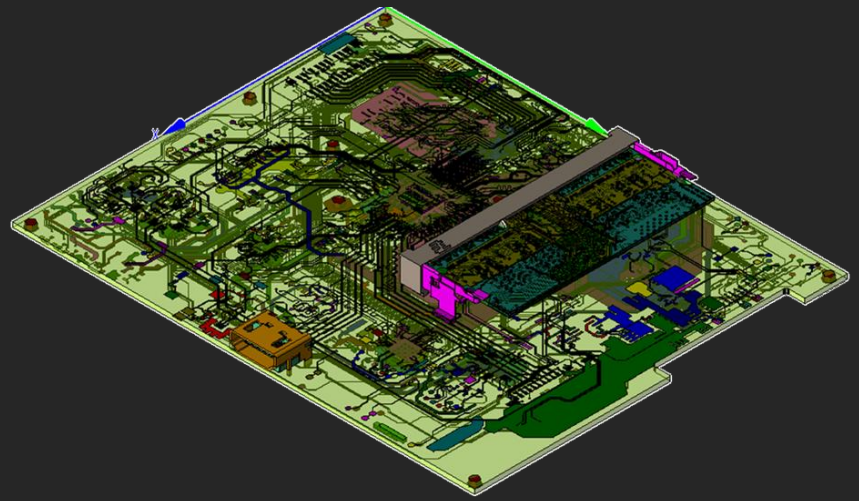




Clarity 3D Solver

For 3D electromagnetic analysis of electronics

- Higher performing electronics require fast and accurate 3D electromagnetic (EM) simulation as complexity increases
- Speed/accuracy of EM for in-design analysis and final system signoff
  - >10x speed up via fast and efficient distributed solver and mesh algorithms
  - Near linear scaling delivers unmatched capacity
  - Integrated workflows with schematic/layout of Allegro® X PCB and APD platforms, AWR® RF software and Virtuoso® Studio
- POR at multiple NASDAQ 100 firms delivering faster TAT on most challenging designs; >100 new logos in 2024
- Used for IC, advanced IC packaging, PCB, and more



Simulation	Legacy (Hrs)	Clarity (Hrs)	Speed Up
Interposer	12	2.25	5.3X
SiP Signal Chain	27	1.5	17.0X
Serdes Package	22.5	2.25	7.0X
HBM Wafer Level SiP	86.4	7.2	12.2X

Conclusion

- Advanced packaging (high-density fan-out package structures) increases design complexity with more high-speed signals, challenging traditional workflows, and deadlines
- Cadence's new methodology enables early, iterative IC package optimization, eliminating delays and lengthy simulation setups
- In-design and signoff analysis with scalable multiphysics engines helps engineers speed up design cycles and manage complex redesigns efficiently

Design / Analysis Technology	Application
Allegro® X APD	IC package design (Now Auto Substrate Route Option)
Sigrity™ X Aurora IC Package Analysis	IC package in-design analysis
Sigrity X XcitePI™, Clarity™ 3D Solver	ICP /silicon interposer interconnect model extraction
Sigrity X XtractIM™ and Clarity 3D Solver	IC package interconnect model extraction
Sigrity X Advanced SI, Sigrity X Advanced PI, and Celsius™ Studio	Signal, power, and thermal integrity signoff